
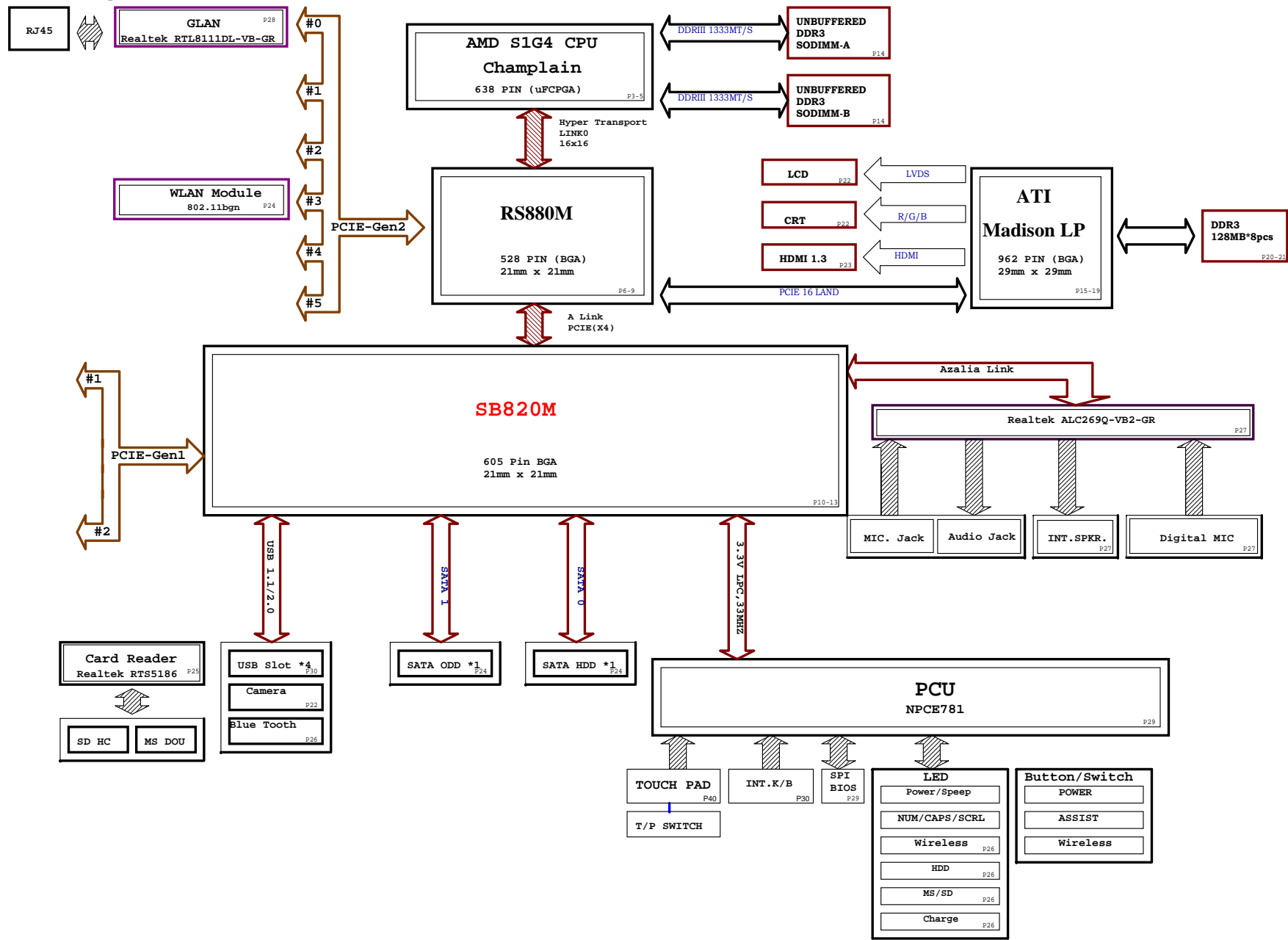


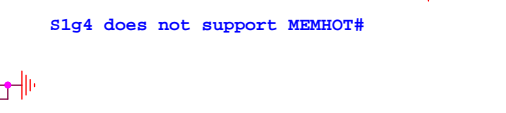
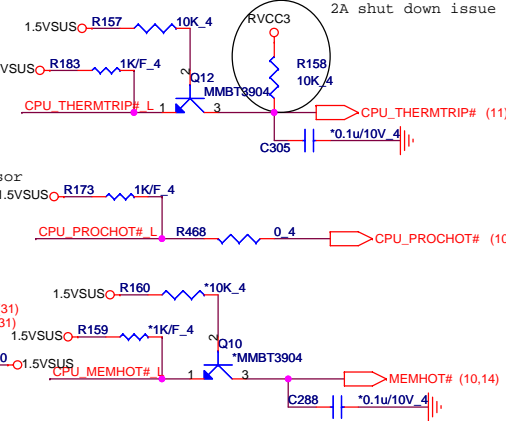
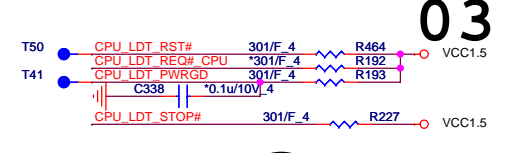
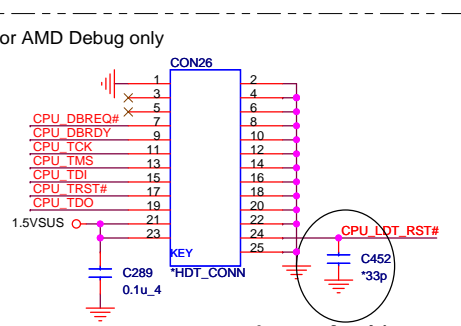
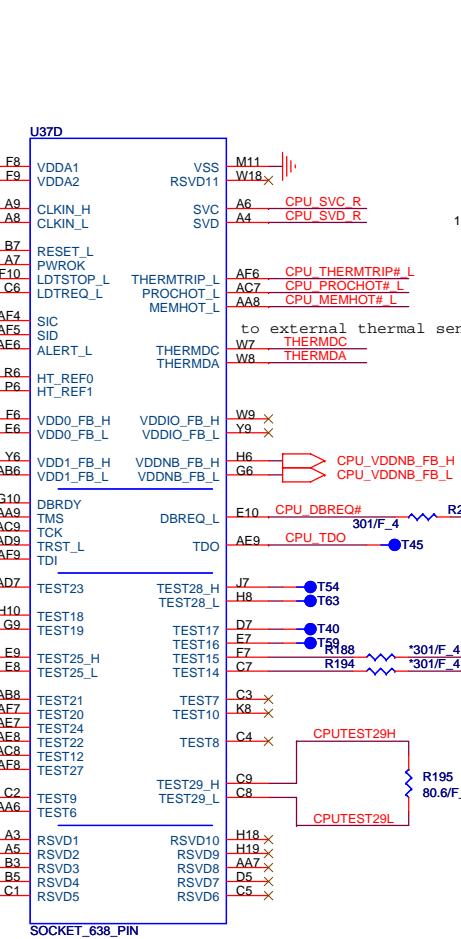
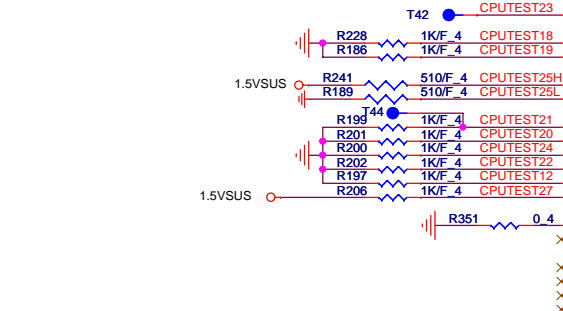
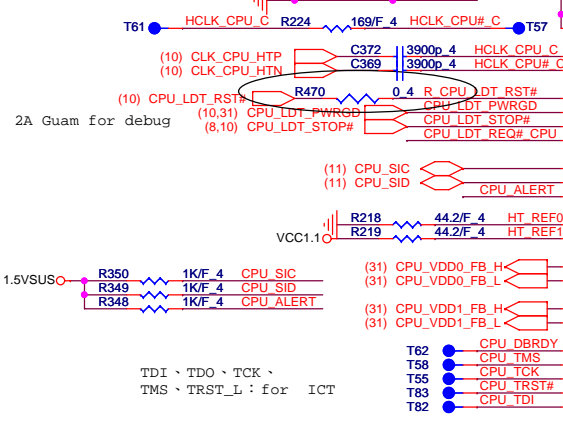
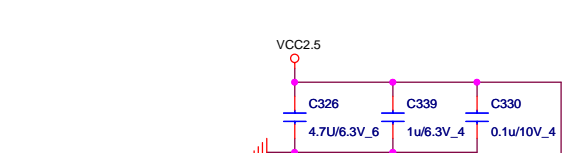
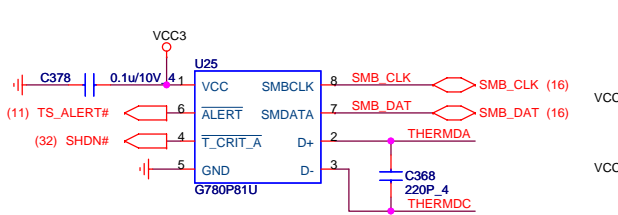
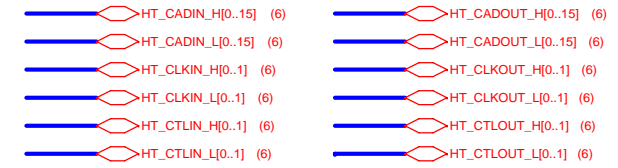
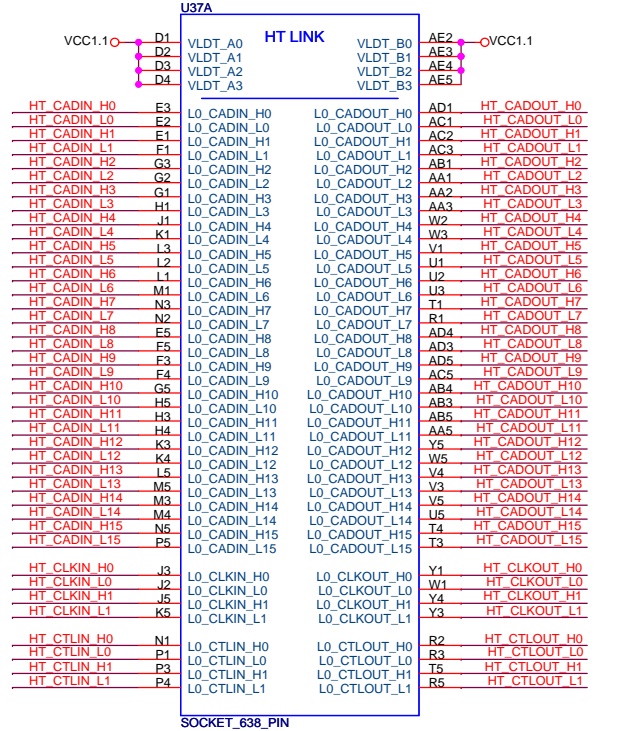
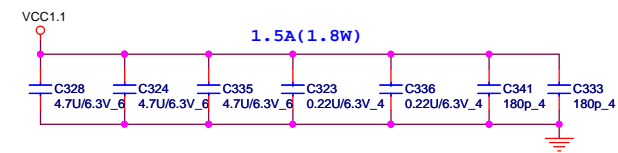
| Page | Title of schematic page            | Rev. | Date  |
|------|------------------------------------|------|-------|
| 01   | Page List                          | 2A   | 12/24 |
| 02   | Block Diagram                      | 2A   | 12/24 |
| 03   | CPU-Champlain HT/CONTROL (1/3)     | 2A   | 01/04 |
| 04   | CPU-Champlain MEMORY (2/3)         | 1B   | 12/16 |
| 05   | CPU-Champlain POWER/GND (3/3)      | 1B   | 12/08 |
| 06   | NB-RS880M HT/SP-MEM (1/4)          | 1B   | 12/08 |
| 07   | NB-RS880M GFX/PCIE (2/4)           | 1A   | 09/24 |
| 08   | NB-RS880M SYSTEM (3/4)             | 1A   | 09/24 |
| 09   | NB-RS880M POWER (4/4)              | 1A   | 09/24 |
| 10   | SB-SB820M PCI/CLK/LPC (1/4)        | 1A   | 09/24 |
| 11   | SB-SB820M AUDIO/USB (2/4)          | 1A   | 09/24 |
| 12   | SB-SB820M SATA (3/4)               | 1B   | 12/08 |
| 13   | SB-SB820M POWER (4/4)              | 1A   | 09/24 |
| 14   | DDR3 SODIMM* 2 (5.2mm+9.2mm)       | 2A   | 12/24 |
| 15   | ATI-Madison LP PCIE/LVDS (1/5)     | 2A   | 12/24 |
| 16   | ATI-Madison LP MAIN I/O (2/5)      | 2A   | 12/24 |
| 17   | ATI-Madison LP POWER/GND (3/5)     | 2A   | 12/24 |
| 18   | ATI-Madison LP Display POWER (4/5) | 2A   | 12/24 |
| 19   | ATI-Madison LP MEM I/F (5/5)       | 2A   | 12/24 |
| 20   | ATI-Madison LP (DDR3 V-ram a)      | 2A   | 12/24 |
| 21   | ATI-Madison LP (DDR3 V-ram b)      | 1B   | 12/08 |
| 22   | CRT/LVDS                           | 2A   | 12/24 |

| Page | Title of schematic page    | Rev. | Date  |
|------|----------------------------|------|-------|
| 23   | HDMI                       | 1B   | 12/09 |
| 24   | WLAN/HDD/ODD               | 1B   | 12/08 |
| 25   | Card Reader RTS5186        | 1B   | 12/08 |
| 26   | Express Card/BT/LED        | 1B   | 12/08 |
| 27   | Codec-ALC269Q VB5 GR       | 1B   | 12/08 |
| 28   | LAN RTL8111E               | 1B   | 12/08 |
| 29   | NPCE781                    | 1B   | 12/08 |
| 30   | KB/USB/FAN/PS              | 1B   | 12/09 |
| 31   | VCORE(ISL6265A)            | 1A   | 09/24 |
| 32   | 3VPCU&5VPCU(PM6686)        | 1A   | 09/24 |
| 33   | 1.5VSUS/VTM_MEM            | 1A   | 09/24 |
| 34   | DYN_VCC1.1(OZ8116LN)       | 1A   | 09/24 |
| 35   | VCC1.1(OZ8116LN)-7A        | 1A   | 09/24 |
| 36   | VGA_CORE(OZ8116)-16A       | 1A   | 09/24 |
| 37   | VCC1.8/0.9/2.5/1.0         | 1A   | 09/24 |
| 38   | POWER(BAT IN / ADA IN/ UL) | 1A   | 09/24 |
| 39   | CHARGER (ISL6252A)         | 1A   | 09/24 |
| 40   | Small board connector      | 1A   | 09/24 |
| 41   | Power Sequence             |      |       |
| 42   | CHANGE LIST                |      |       |
|      |                            |      |       |
|      |                            |      |       |

1.Level 1 Environment-related Substances Should NEVER be Used.  
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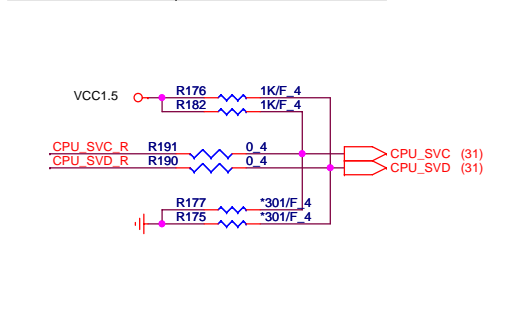
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|-------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|---------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : NE8</b> |                             | Rev<br>2A     |
|                                                                                                                                           |                             |               |
| <b>AMD Danube</b>                                                                                                                         |                             |               |
| Date:                                                                                                                                     | Wednesday, January 27, 2010 | Sheet 1 of 42 |





VFIX MODE VID Override Circuit

| SVC | SVD | Voltage Output |
|-----|-----|----------------|
| 0   | 0   | 1.1V           |
| 0   | 1   | 1.0V           |
| 1   | 0   | 0.9V           |
| 1   | 1   | 0.8V           |



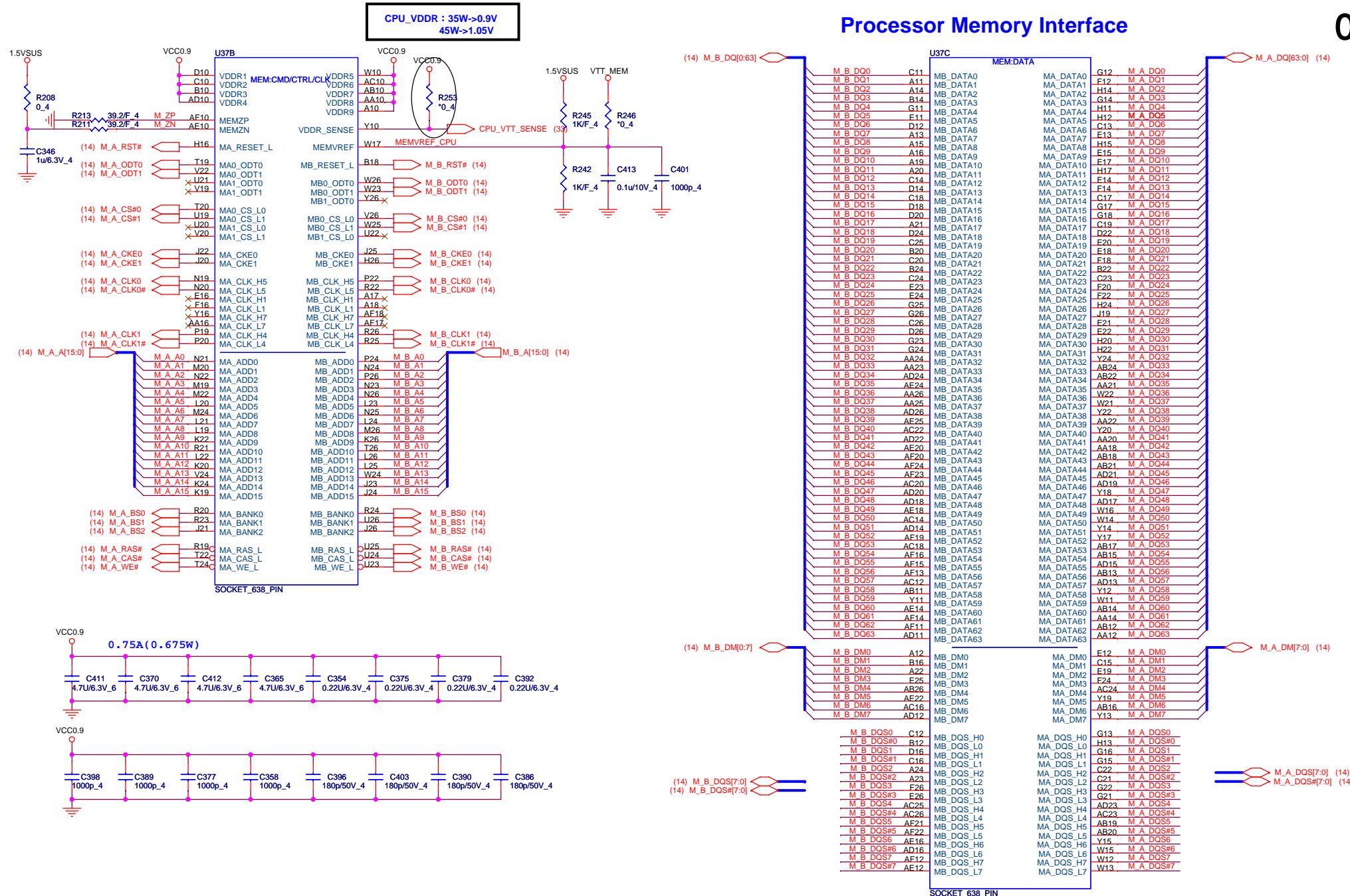
Quanta Computer Inc.

PROJECT : NE8

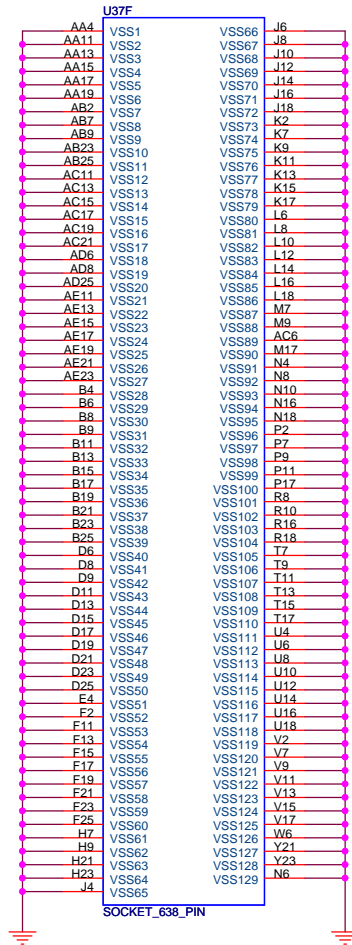
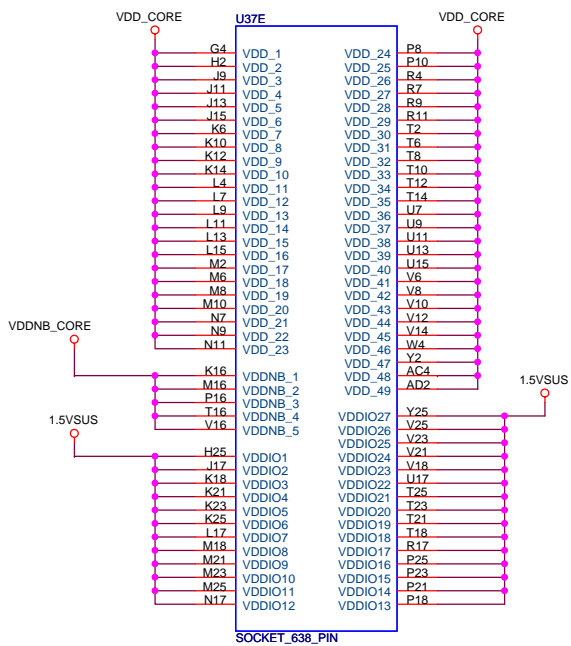
CPU HT/CONTROL(1/3)

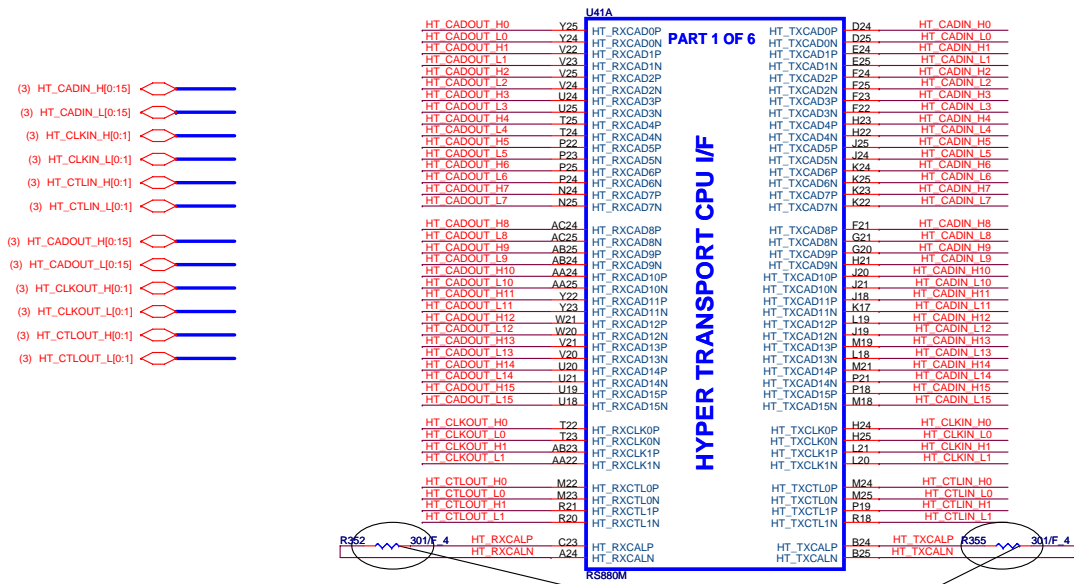
Date: Wednesday, January 27, 2010 Sheet 3 of 42

1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



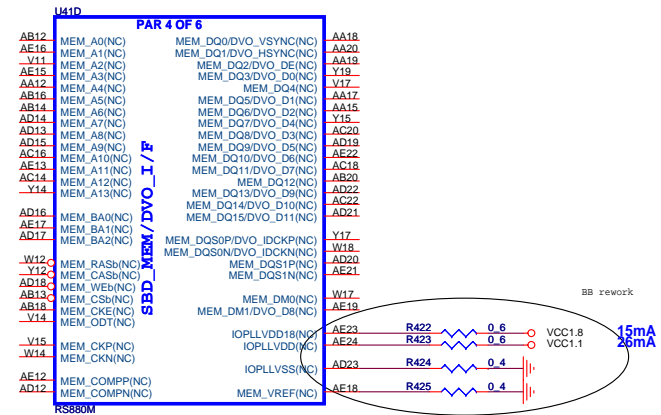
| Socket Type | QCI P/N     |
|-------------|-------------|
| Normal      | DG0^8000018 |
| 90 degree   | DG0^8000023 |



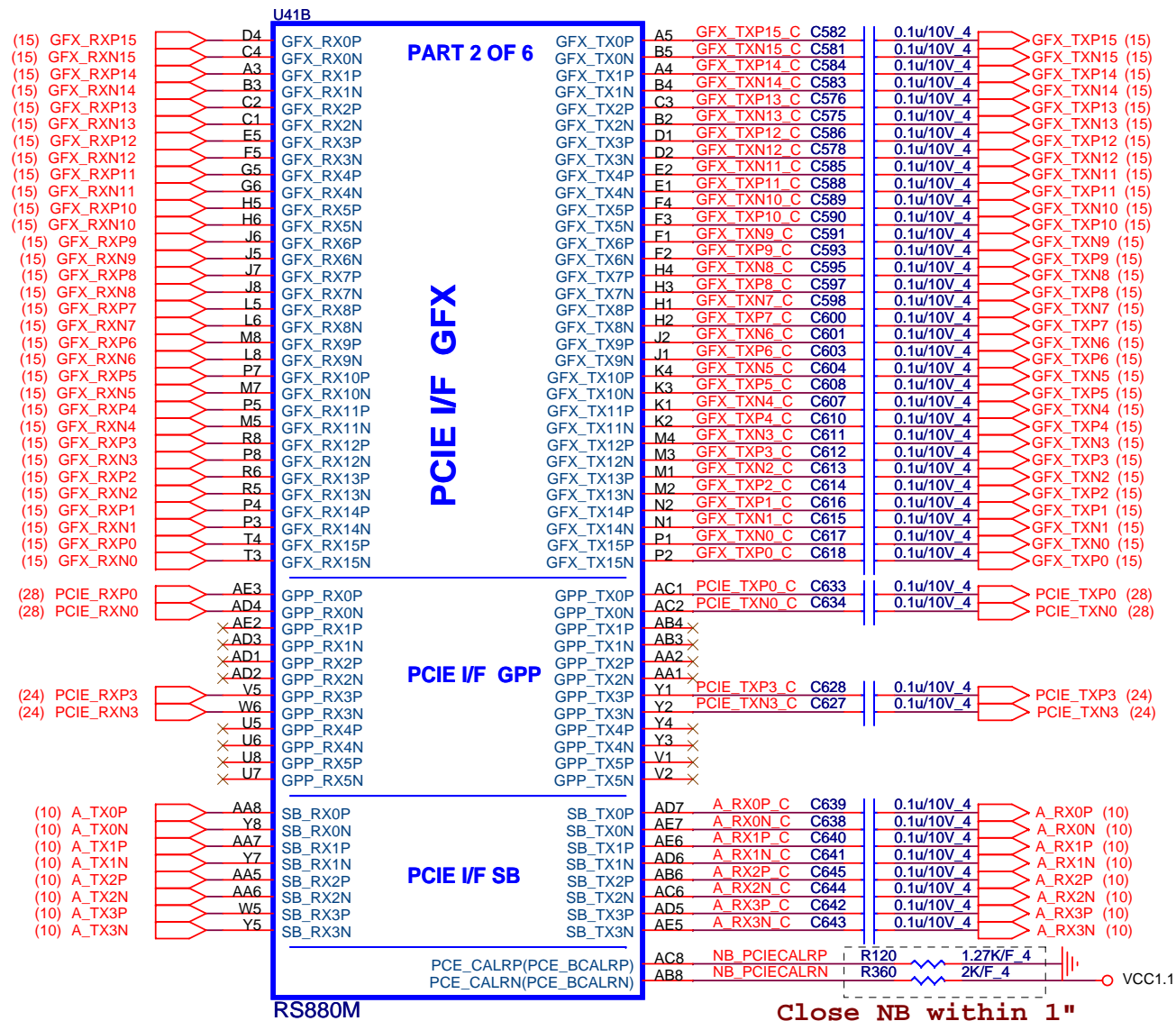


1A: Guam 301 ohm /NBDC 1.21K  
CLK Gen or SB820 mount different.

This block is for Side Port only , others can remove some components







Layout Swap  
 TX11, TX10, TX9,  
 TX8, TX7, TX6, TX5,  
 TX4, TX3, TX2, TX0

GLAN

WLAN

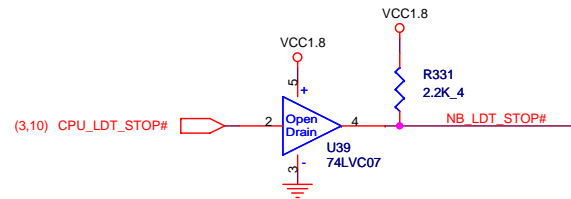
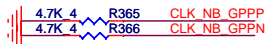
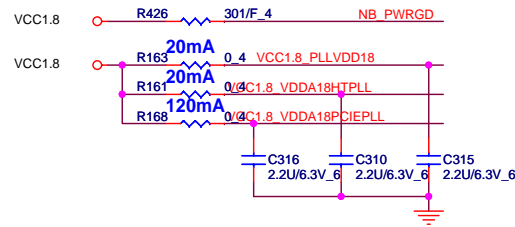
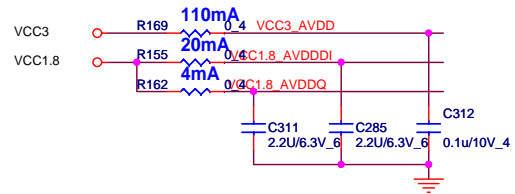


**Quanta Computer Inc.**

**PROJECT : NE8**

|       |                             |               |
|-------|-----------------------------|---------------|
| Size  | Document Number             | Rev           |
|       | <b>RS880M GFX/PCIE(2/4)</b> | 2A            |
| Date: | Wednesday, January 27, 2010 | Sheet 7 of 42 |

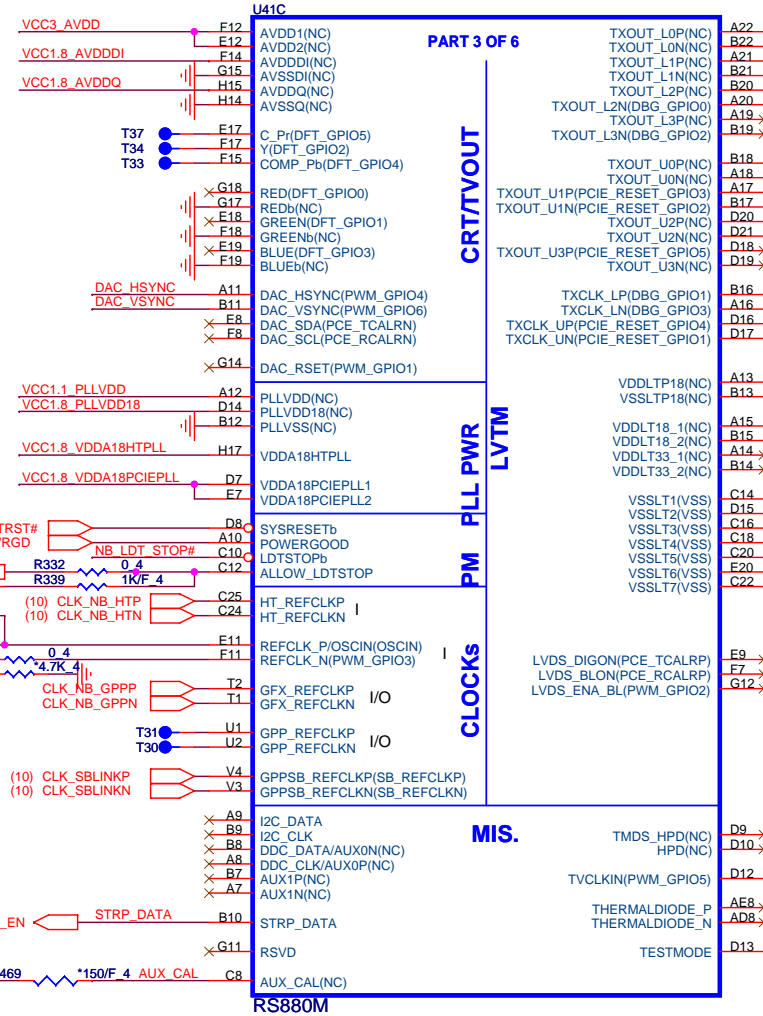
- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.




Enables Debug Bus access through memory I/O pads and GPIO.  
0 : Enable RS880M , Default  
1 : Disable RS880M

Discrete : Connect All, B11

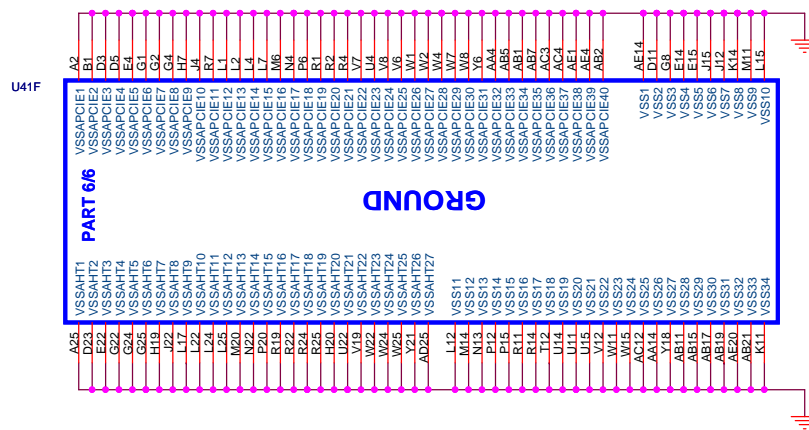
Indicates if memory Side port is available or not  
1: Disable side port memory  
0: Enable side port memory



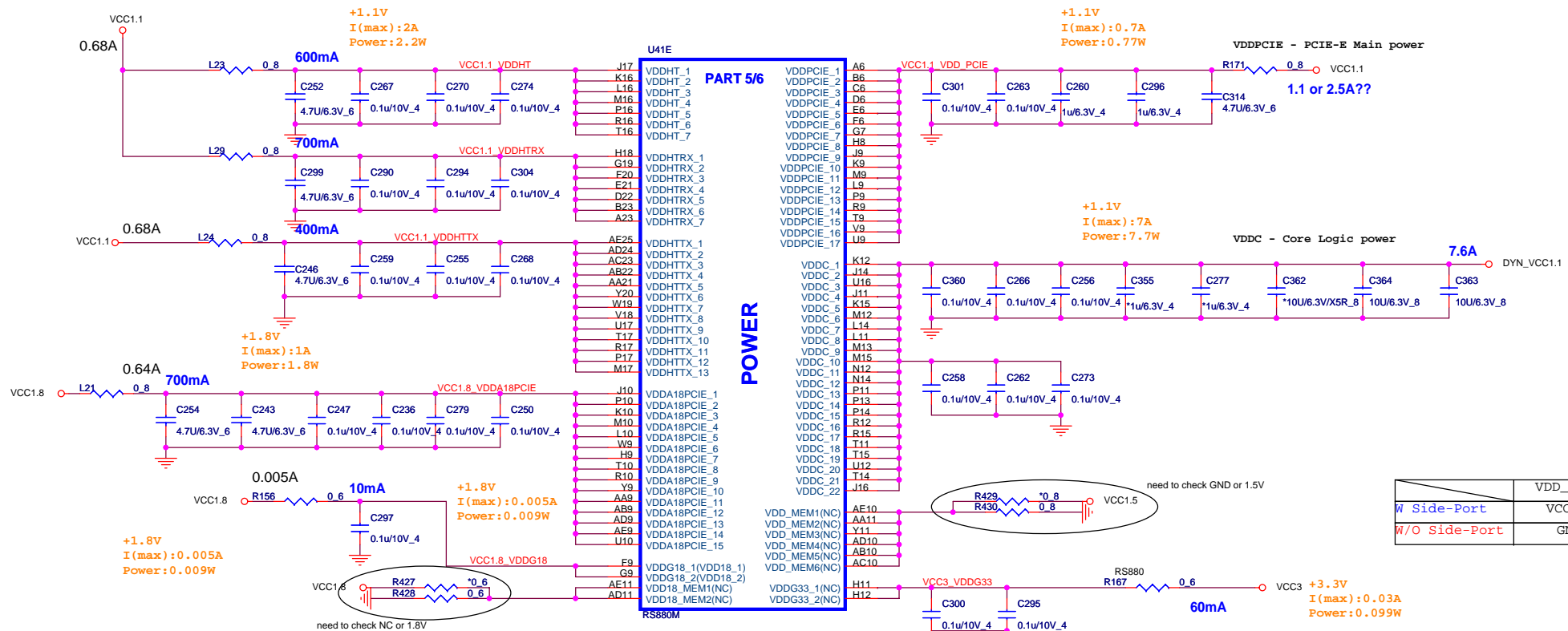
1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

|                                                                                                                                           |                             |               |
|-------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|---------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : NE8</b> |                             | Rev<br>2A     |
|                                                                                                                                           |                             |               |
| <b>RS880M SYSTEM(3/4)</b>                                                                                                                 |                             |               |
| Date:                                                                                                                                     | Wednesday, January 27, 2010 | Sheet 8 of 42 |





| RS880M/RX881 POWER DIFFERENCE TABLE |       |        |               |       |        |
|-------------------------------------|-------|--------|---------------|-------|--------|
| PIN NAME                            | RX881 | RS880M | PIN NAME      | RX881 | RS880M |
| VDDHT                               | +1.1V | +1.1V  | IOPLLVD       | NC    | +1.1V  |
| VDDHTRX                             | +1.1V | +1.1V  | AVDD          | NC    | +3.3V  |
| VDDHTTX                             | +1.1V | +1.1V  | AVDDDI        | NC    | +1.8V  |
| VDDA18PCIE                          | +1.8V | +1.8V  | AVDDQ         | NC    | +1.8V  |
| VDDG18                              | +1.8V | +1.8V  | PLLVD         | NC    | +1.1V  |
| VDD18_MEM                           | NC    | +1.8V  | PLLVD18       | NC    | +1.8V  |
| VDDPCIE                             | +1.1V | +1.1V  | VDDA18PCIEPLL | +1.8V | +1.8V  |
| VDDC                                | +1.1V | +1.1V  | VDDA18HTPLL   | +1.8V | +1.8V  |
| VDD_MEM                             | NC    | +1.5V  | VDDLTP18      | NC    | +1.8V  |
| VDDG33                              | NC    | +3.3V  | VDDL18        | NC    | +1.8V  |
| IOPLLVD18                           | NC    | +1.8V  | VDDL18        | NC    | +1.8V  |



|               |         |
|---------------|---------|
|               | VDD_MEM |
| W Side-Port   | VCC1.5  |
| W/O Side-Port | GND     |

|               |           |
|---------------|-----------|
|               | VDD18_MEM |
| W Side-Port   | VCC1.8    |
| W/O Side-Port | GND       |

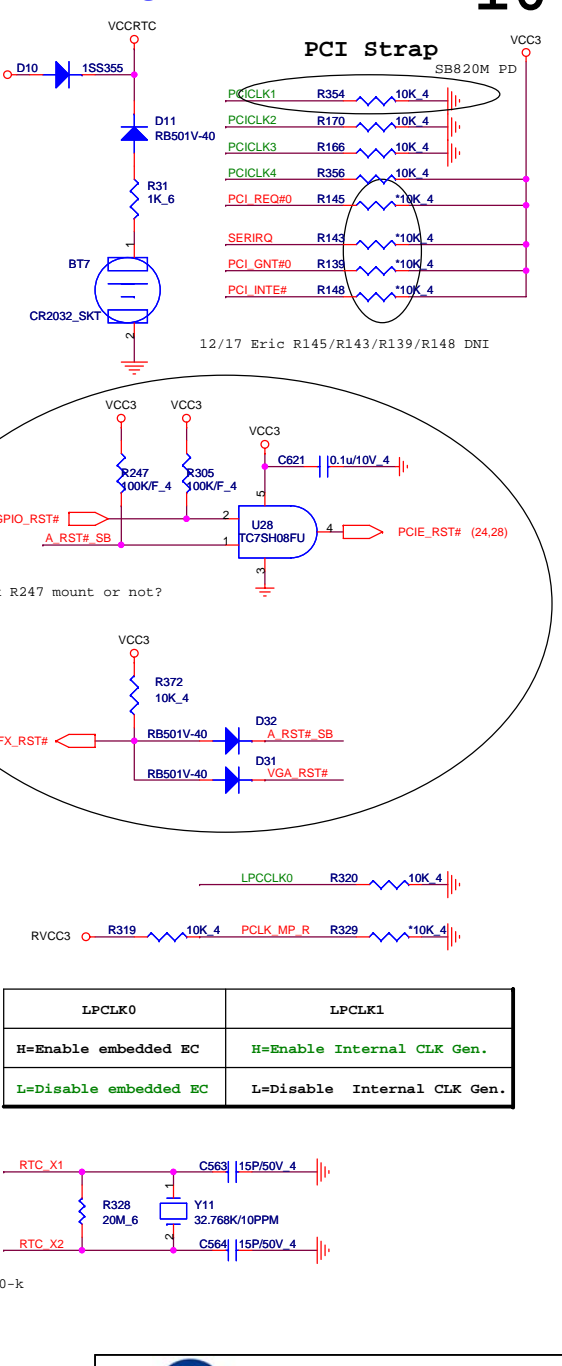
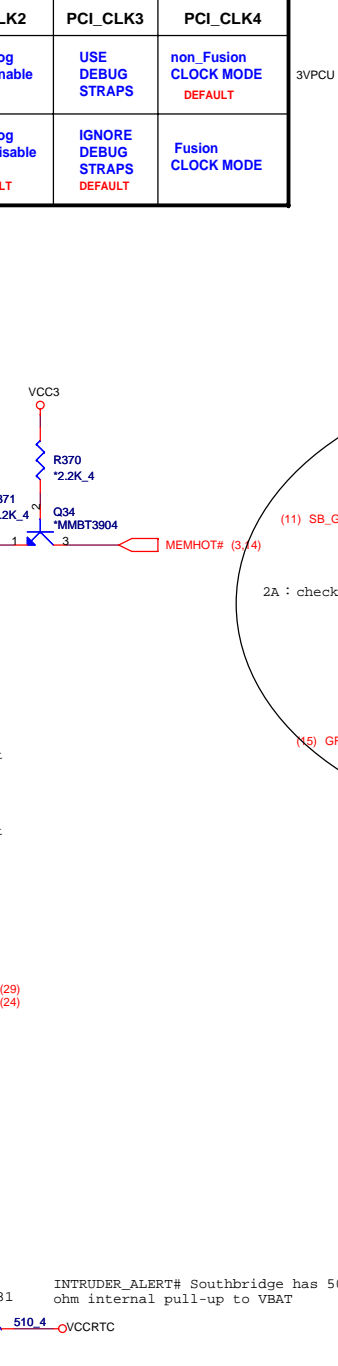
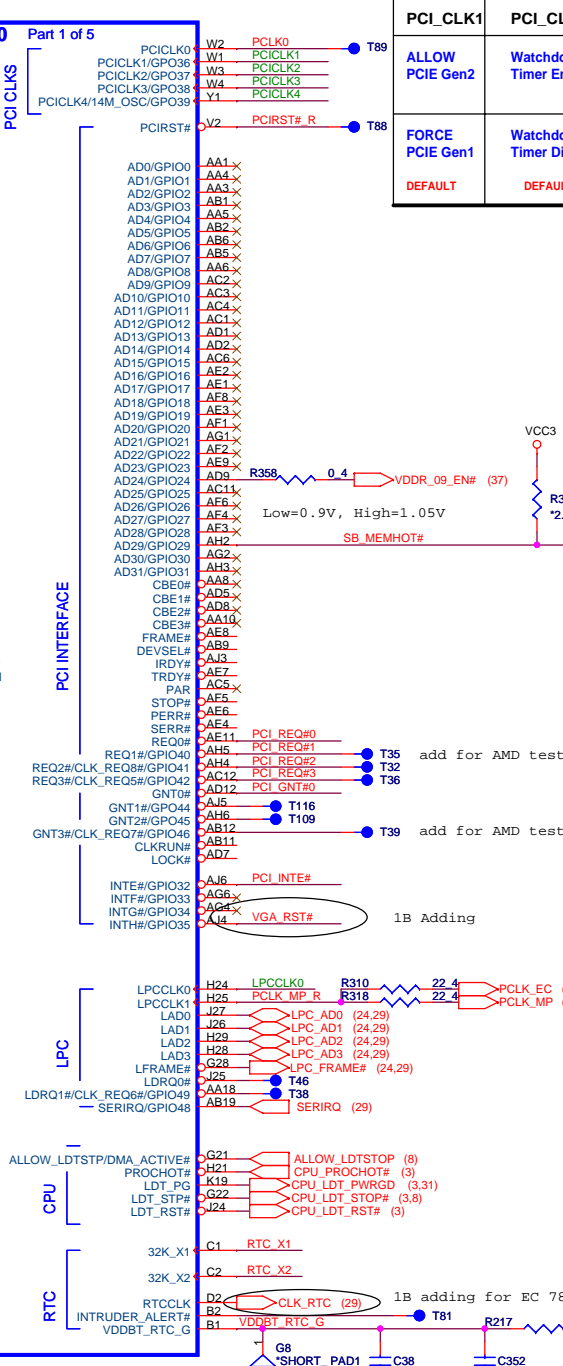
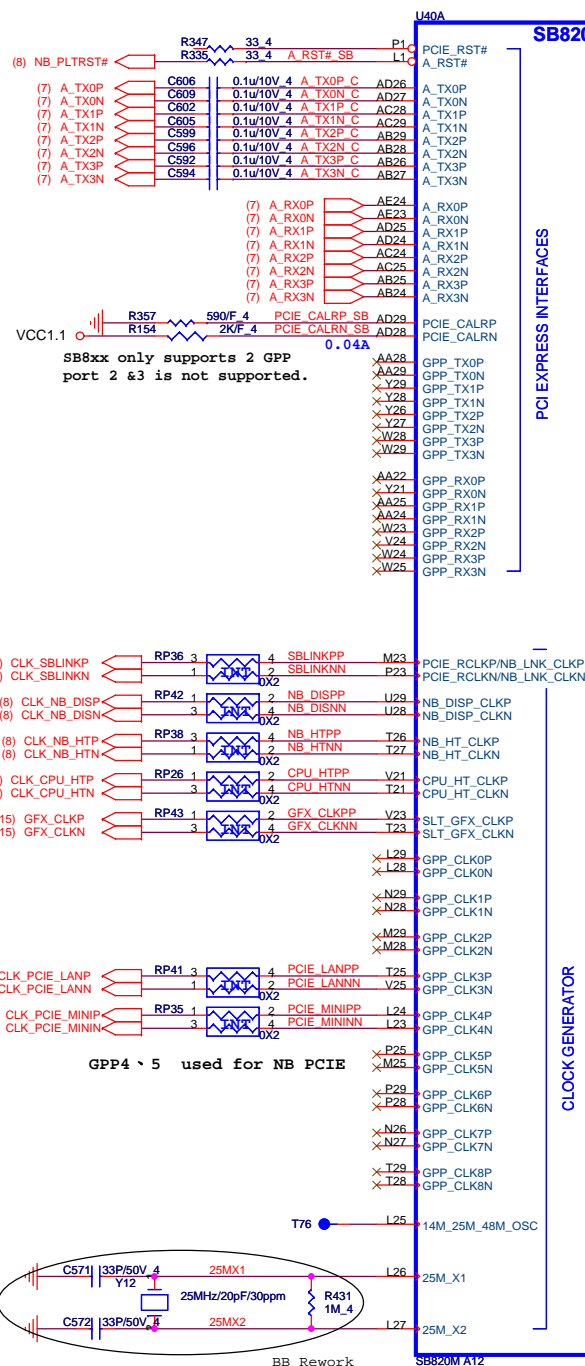
1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

# Strap Table

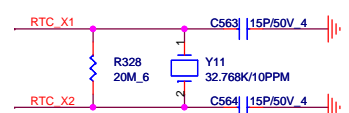
| PCI_CLK1           | PCI_CLK2                  | PCI_CLK3                  | PCI_CLK4                            |
|--------------------|---------------------------|---------------------------|-------------------------------------|
| ALLOW<br>PCIE Gen2 | Watchdog<br>Timer Enable  | USE<br>DEBUG<br>STRAPS    | non_Fusion<br>CLOCK MODE<br>DEFAULT |
| FORCE<br>PCIE Gen1 | Watchdog<br>Timer Disable | IGNORE<br>DEBUG<br>STRAPS | Fusion<br>CLOCK MODE                |
| DEFAULT            | DEFAULT                   | DEFAULT                   |                                     |

RTC

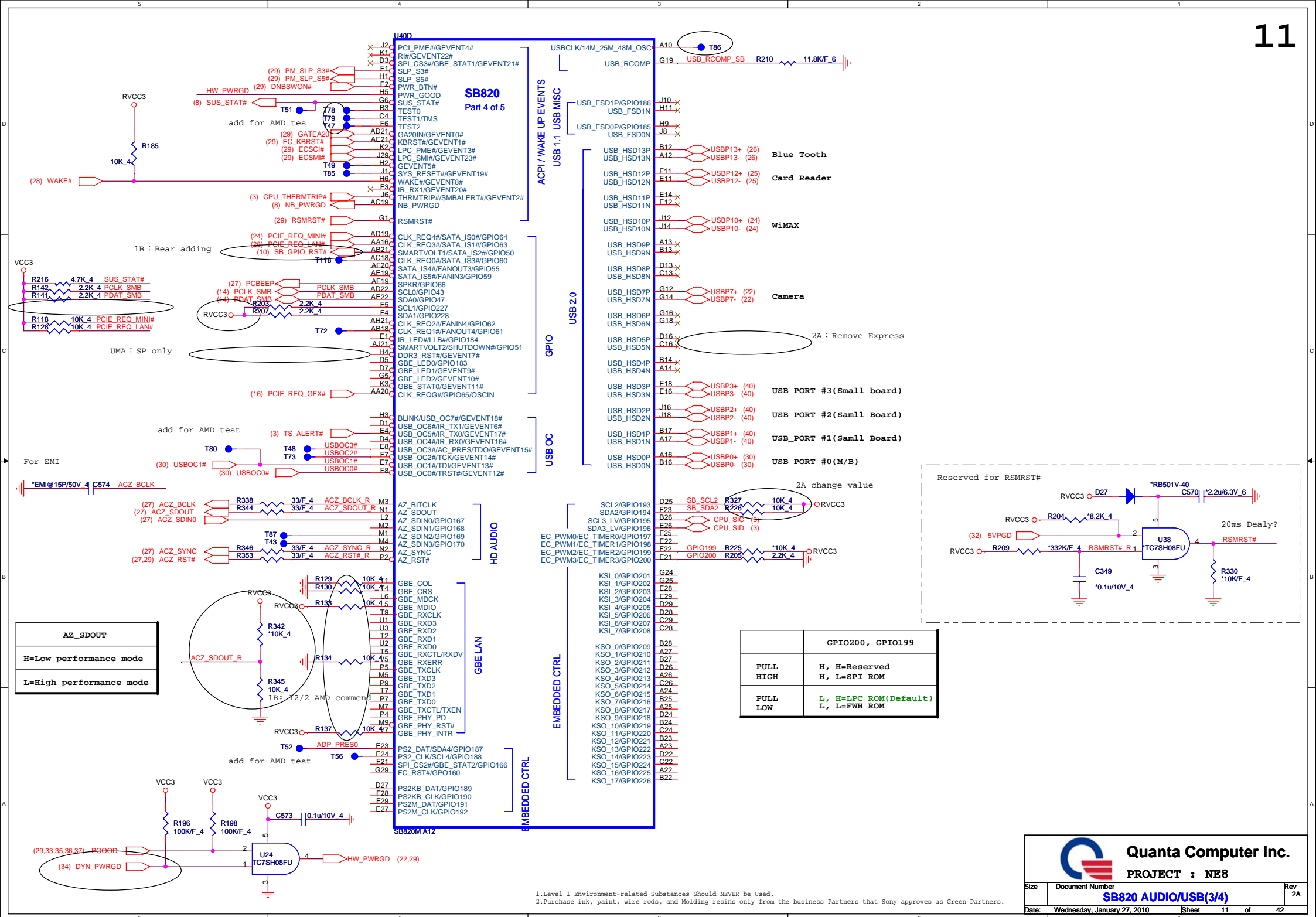
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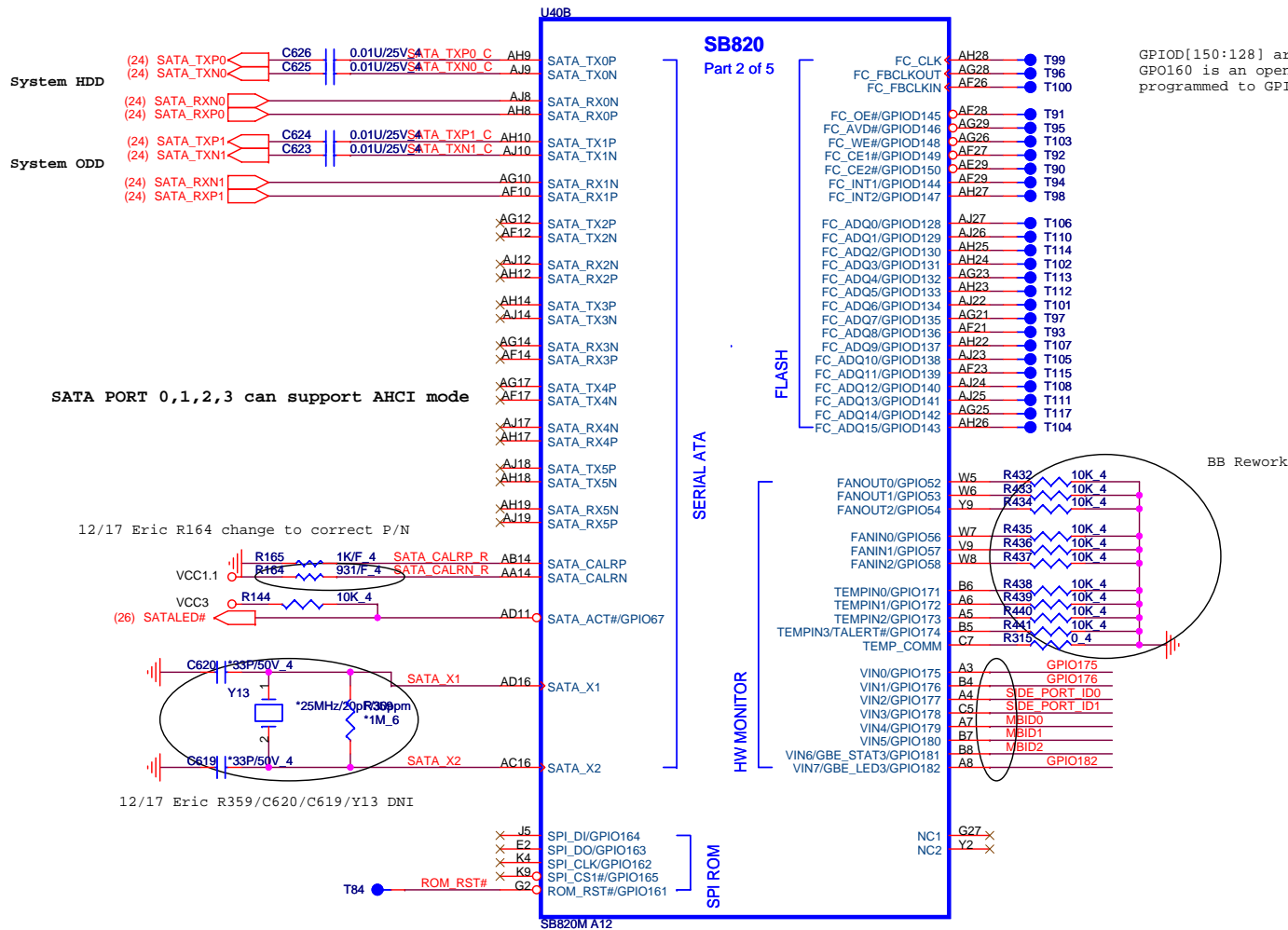
| LPCLK0                | LPCLK1                      |
|-----------------------|-----------------------------|
| H=Enable embedded EC  | H=Enable Internal CLK Gen.  |
| L=Disable embedded EC | L=Disable Internal CLK Gen. |



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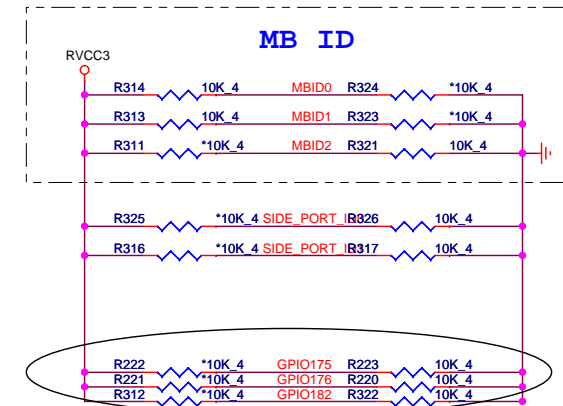
1.Level 1 Environment-related Substances should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.




GPIO[150:128] are open drain GPIO pins where as GP0160 is an open drain GPO pin. These pins are not programmed to GPIO mode by default.

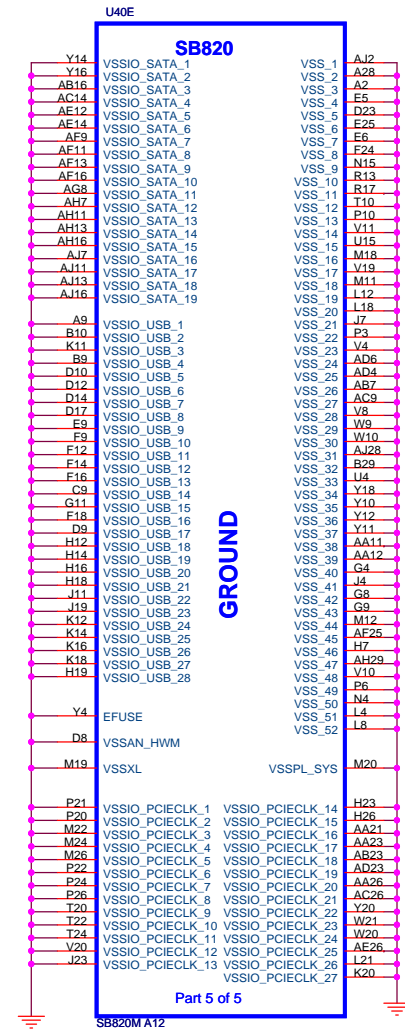
| ID2 | ID1 | ID0 |                      |
|-----|-----|-----|----------------------|
| 0   | 0   | 0   | Danube UMA           |
| 0   | 0   | 1   | Danube UMA+Side port |
| 0   | 1   | 0   | Danube+Park XT       |
| 0   | 1   | 1   | Danube+Madison LP    |
| 1   | 0   | 0   | Danube+M92 XTX       |
| 1   | 0   | 1   |                      |
| 1   | 1   | 0   |                      |
| 1   | 1   | 1   |                      |

|        | NON | SAMSUNG | HYNIX |   |
|--------|-----|---------|-------|---|
| SP ID0 | 0   | 1       | 0     | 1 |
| SP ID1 | 0   | 0       | 1     | 1 |

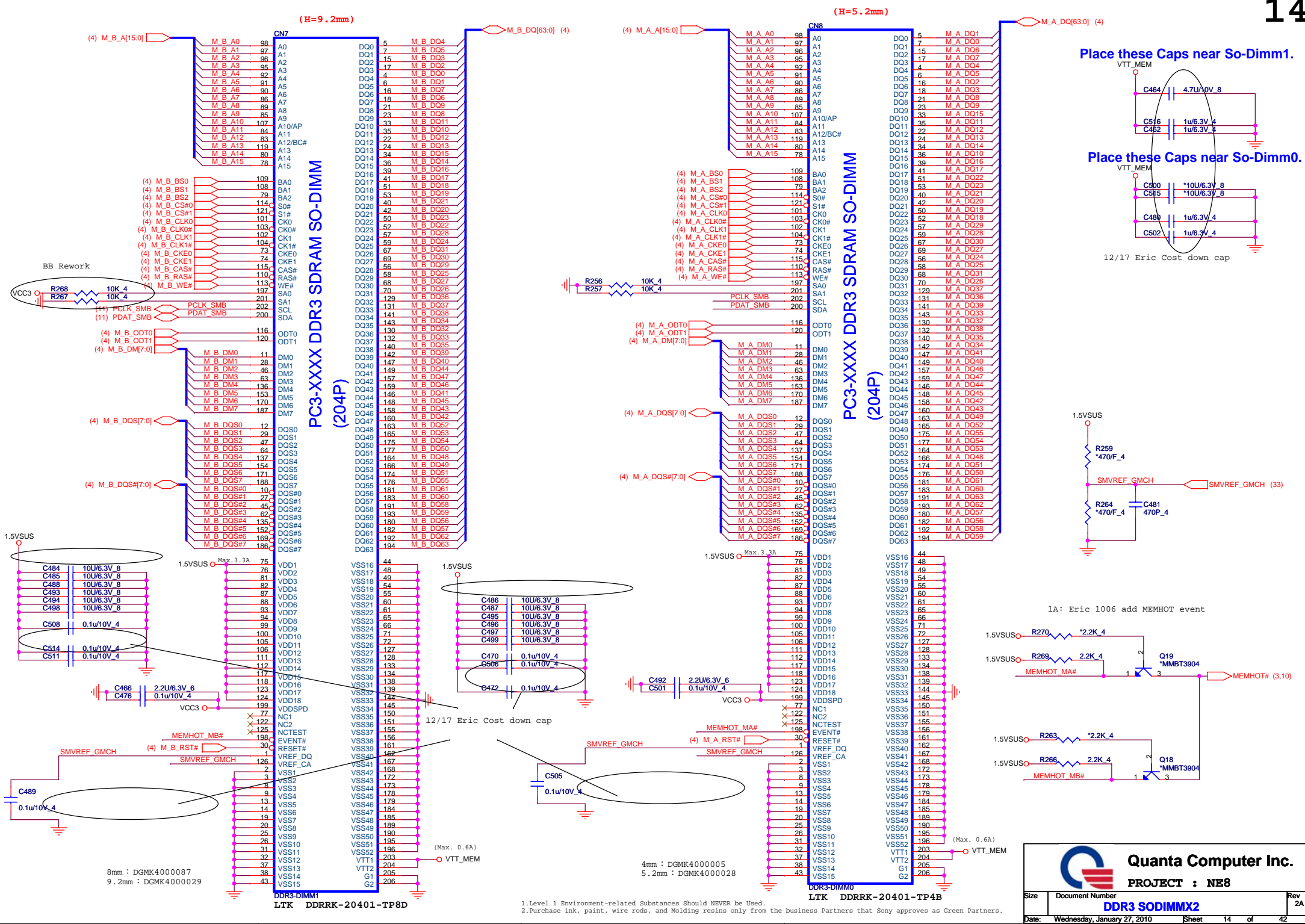


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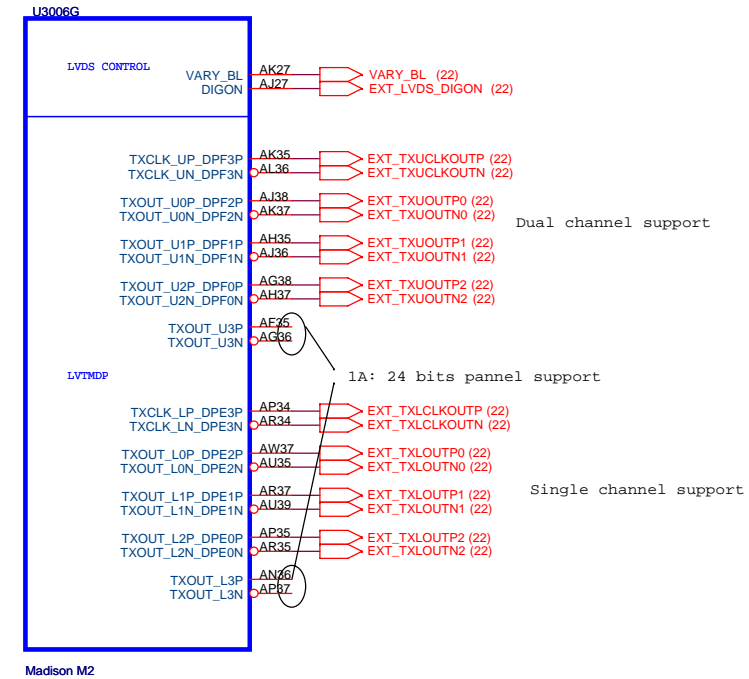
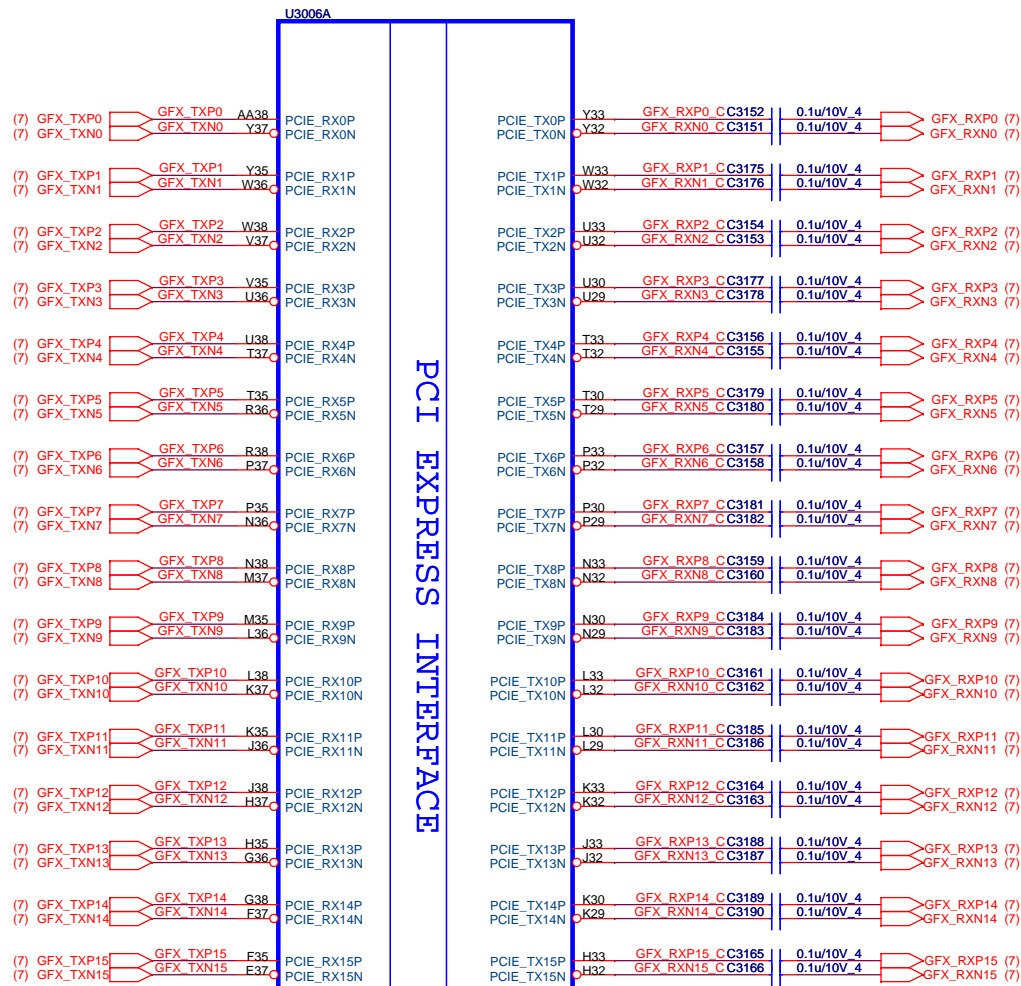
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|  <b>Quanta Computer Inc.</b><br><b>PROJECT : NE8</b> |                             | Size  | Document Number        | Rev   |
|                                                                                                                                           |                             |       | <b>SB820 SATA(2/4)</b> | 2A    |
| Date:                                                                                                                                     | Wednesday, January 27, 2010 | Sheet | 12                     | of 42 |











M9x : R3039 -&gt; NC

1.Level 1 Environment-related Substances Should NEVER be Used.  
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PROJECT : NE8

| Size | Document Number | Rev |
|------|-----------------|-----|
|      | ATI PCIE/LVDS   | 2A  |

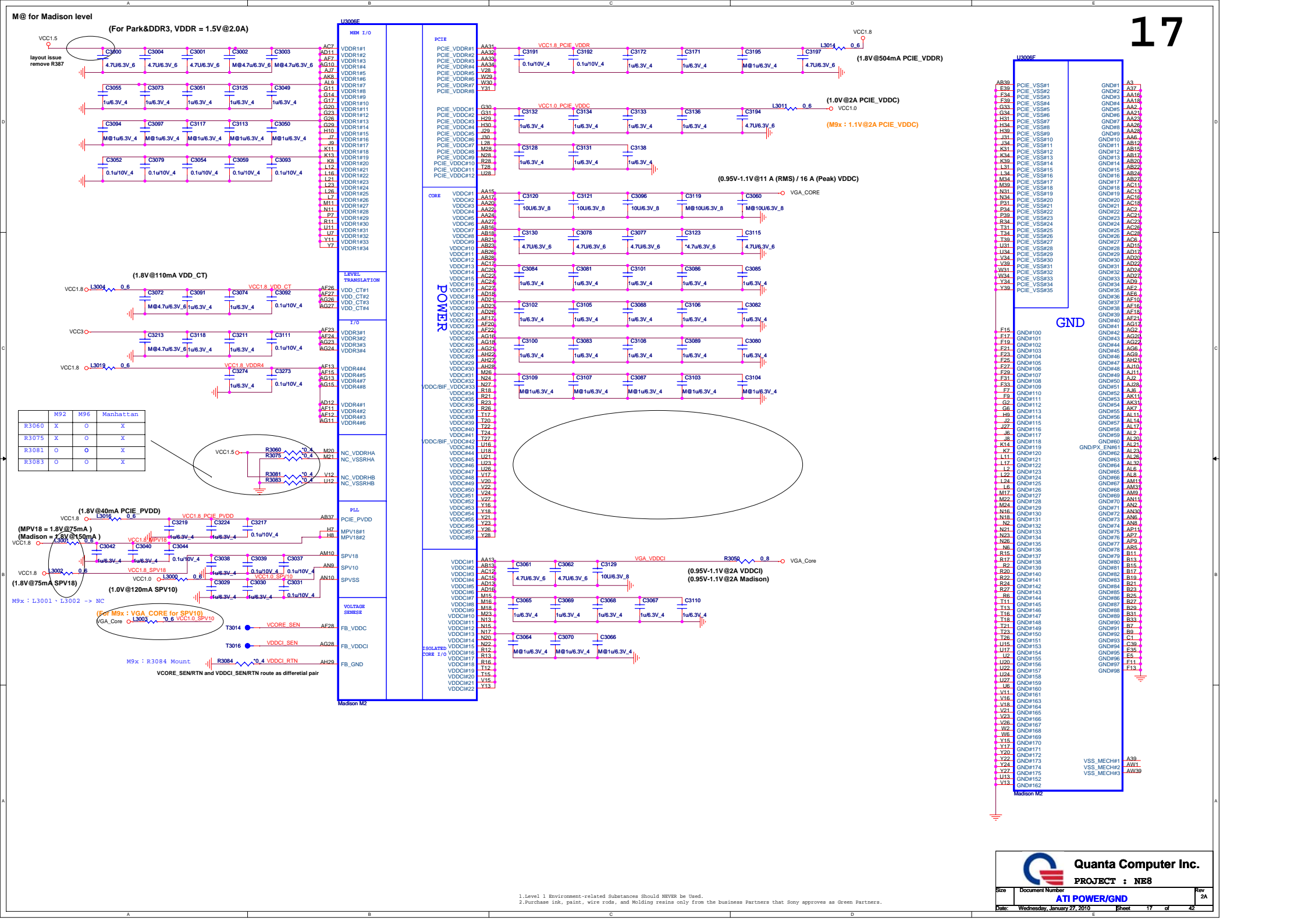
Date: Wednesday, January 27, 2010 Sheet 15 of 42

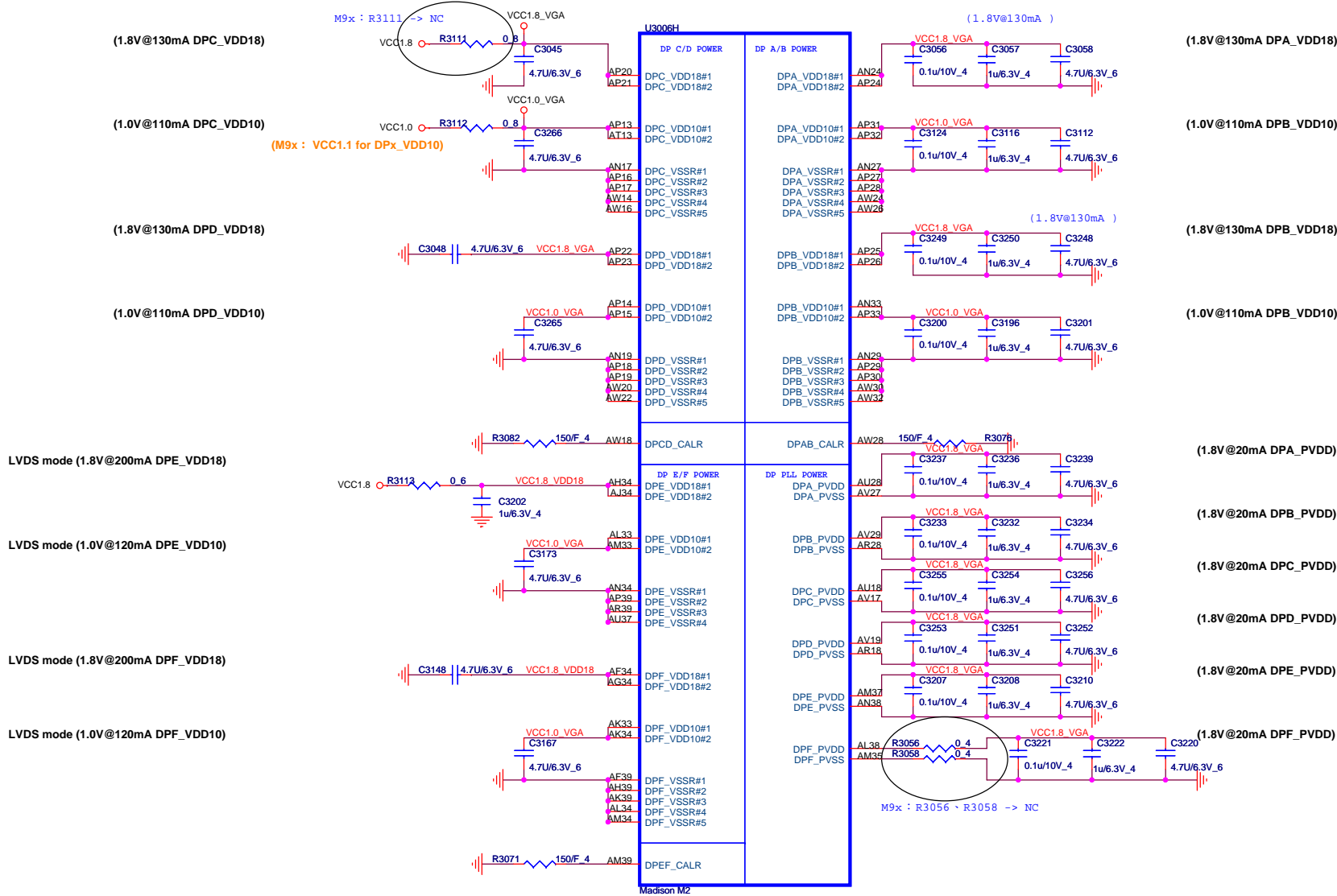


Rev  
2A

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|   |   |
|---|---|
| C | D |
|---|---|





1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Use this option ONLY  
for Park-S3

|                                                                                                                                    |                             |       |                 |     |    |
|------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|-------|-----------------|-----|----|
|  <b>Quanta Computer Inc.</b><br>PROJECT : NE8 |                             | Size  | Document Number | Rev |    |
|                                                                                                                                    |                             | 2A    | ATI MEM/F/DP    | 2A  |    |
| Date:                                                                                                                              | Wednesday, January 27, 2010 | Sheet | 18              | of  | 42 |

# Park Use Channel B Memory Interface Only

## MEMORY INTERFACE A


## MEMORY INTERFACE B

## MEMORY INTERFACE C

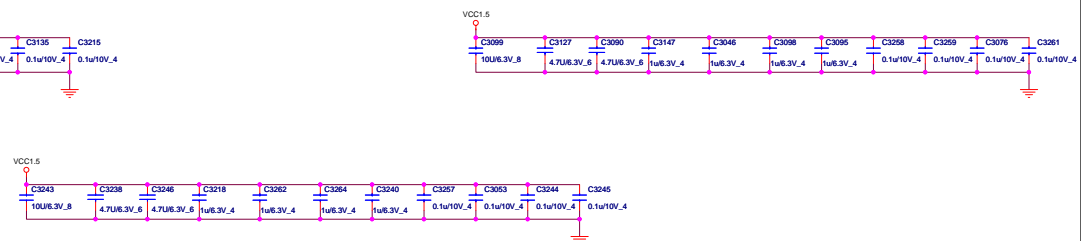
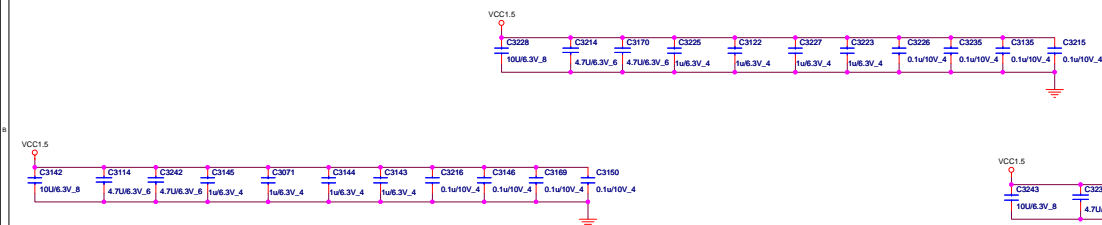
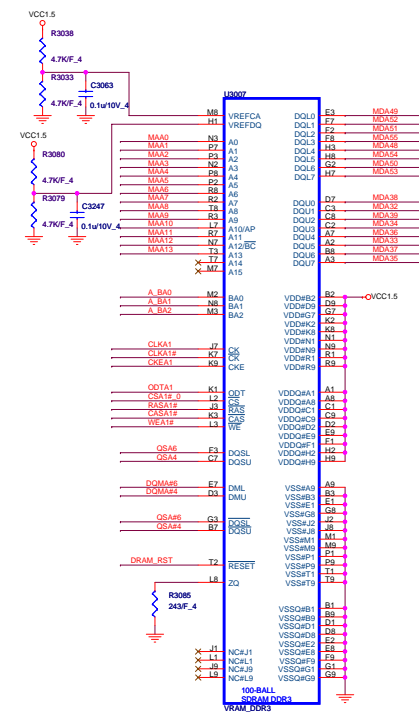
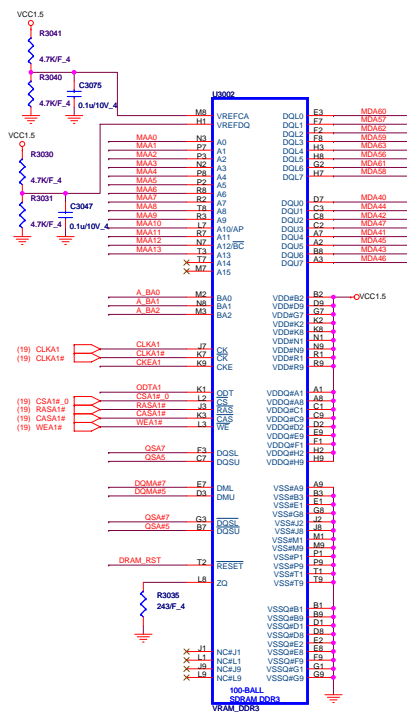
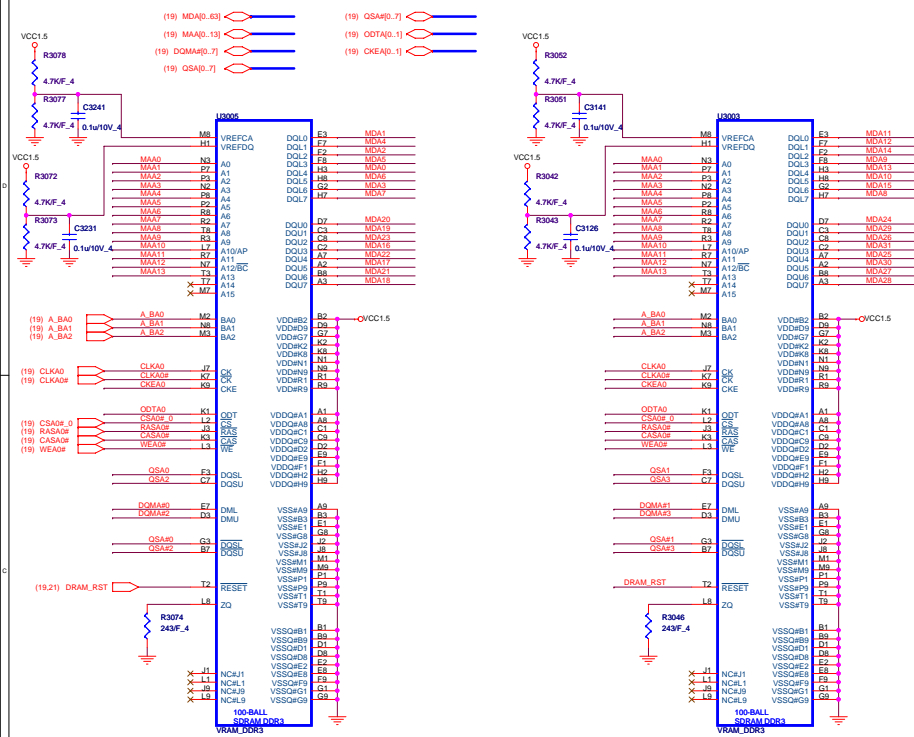
## MEMORY INTERFACE D

|          | DDR3  |
|----------|-------|
| MEM_CALR | 1.5V  |
| Ra       | 40.2R |
| Rb       | 100R  |

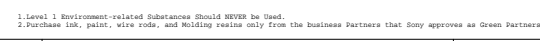
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|                                                                                                                                           |                             |                |
|-------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|----------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : NE8</b> |                             |                |
| Size                                                                                                                                      | Document Number             | Rev            |
|                                                                                                                                           | <b>ATI MEM IF</b>           | <b>2A</b>      |
| Date                                                                                                                                      | Wednesday, January 27, 2010 | Sheet 19 of 42 |

Use this option ONLY  
for Park-S3



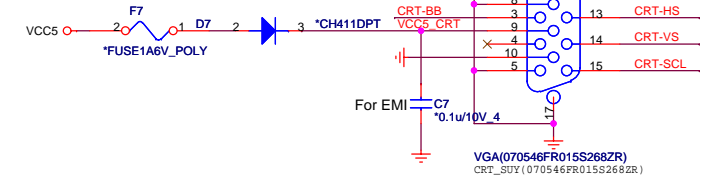
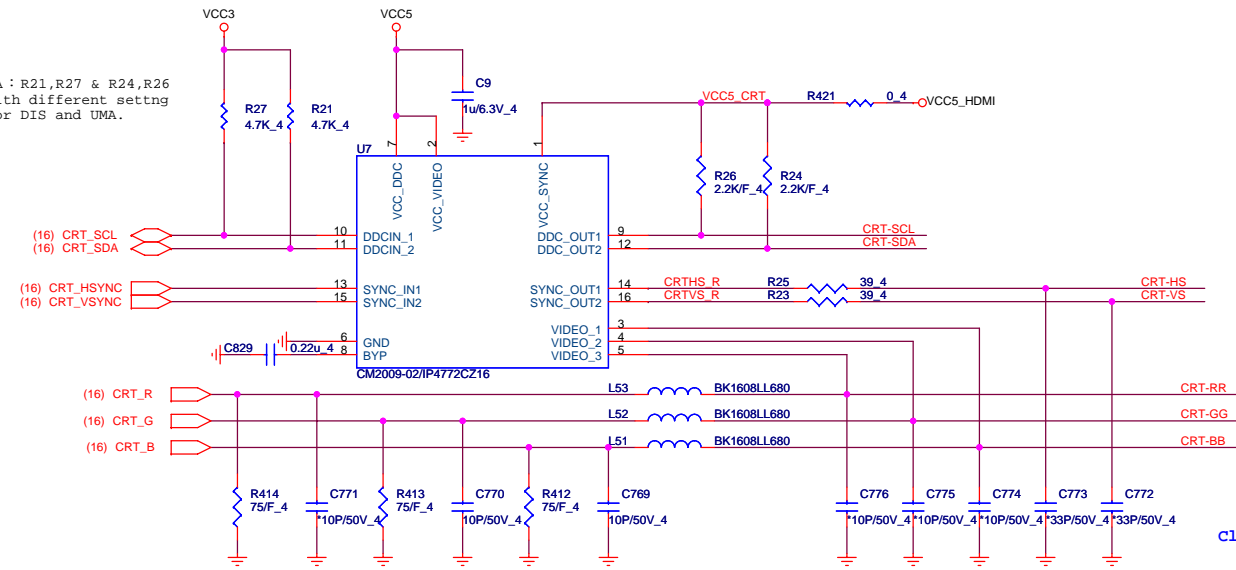




# CRT

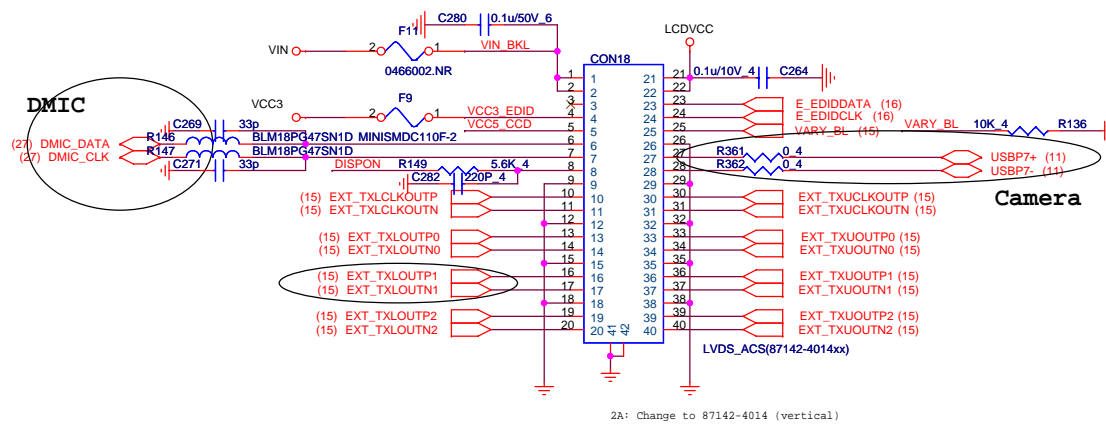
22

2A: R21, R27 & R24, R26 with different setting for DIS and UMA.



Close to Con3

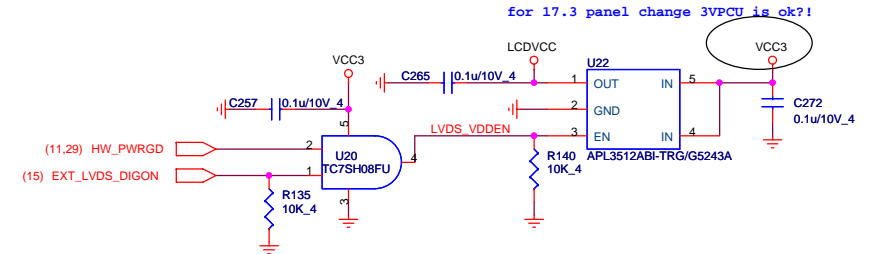
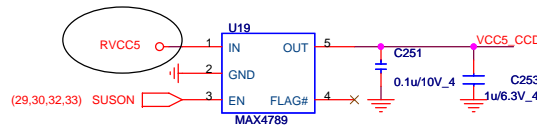
# LVDS



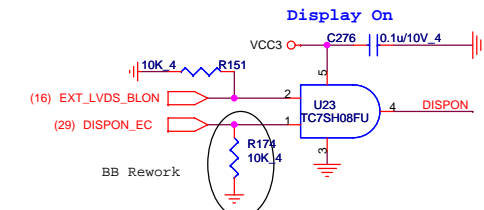
Camera

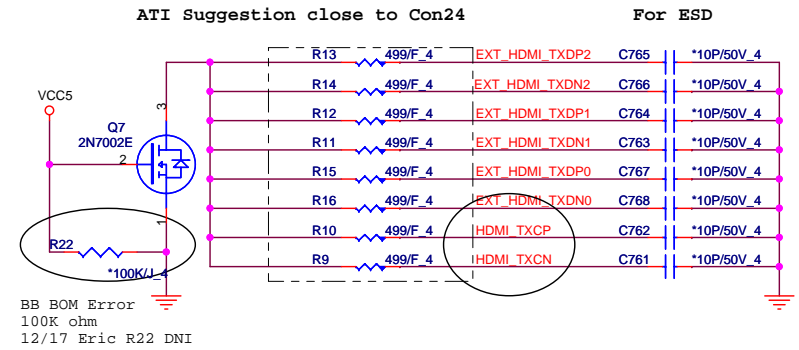
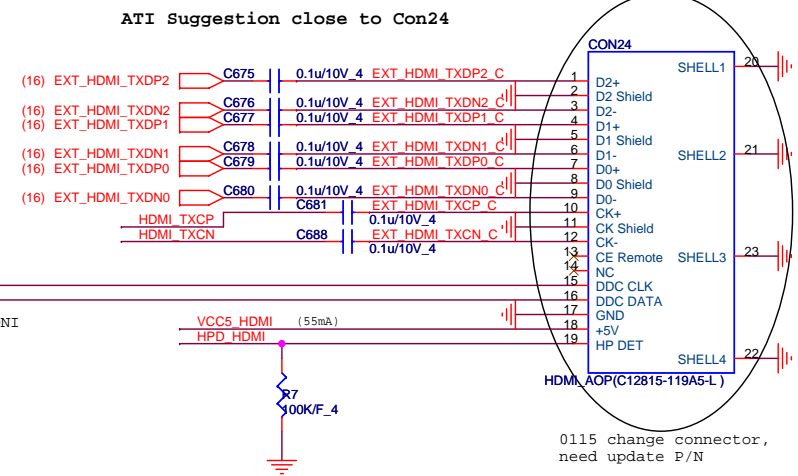
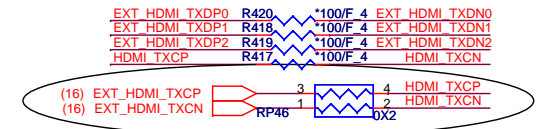
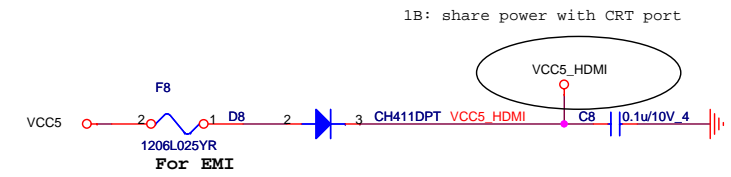
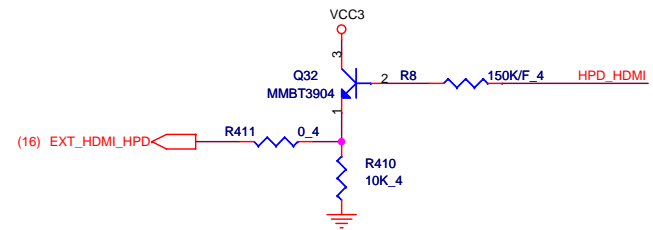
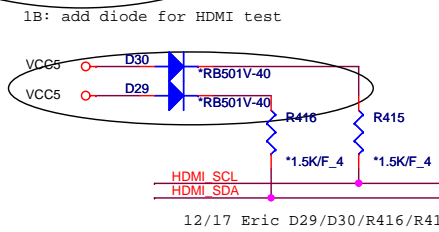
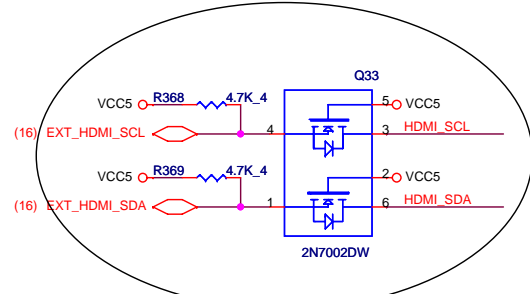
2A: Change to 87142-4014 (vertical)

1C: 12/17 add RVCC5 for optional power source

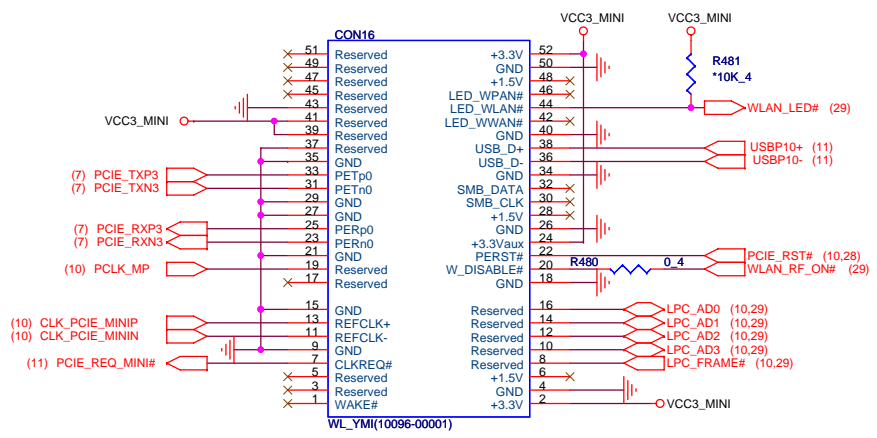


for 17.3 panel change 3VPCU is ok?!

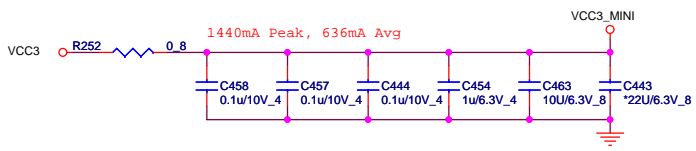




1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

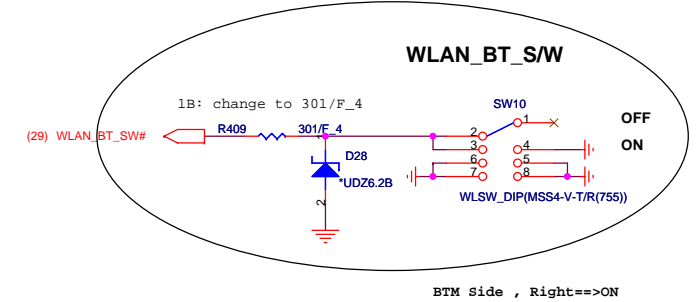


Win7 didn't support wake WLAN

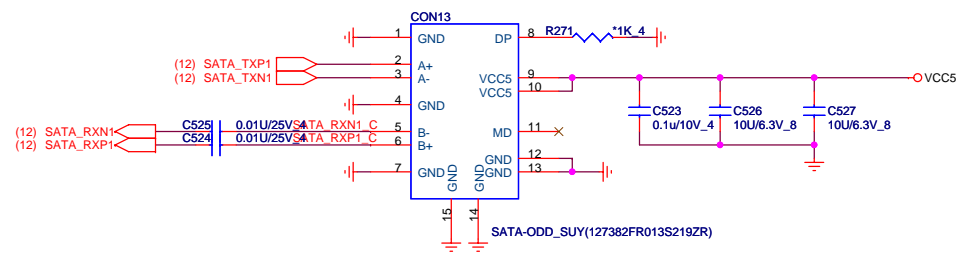


2A : deleted VCC1.5\_MINI

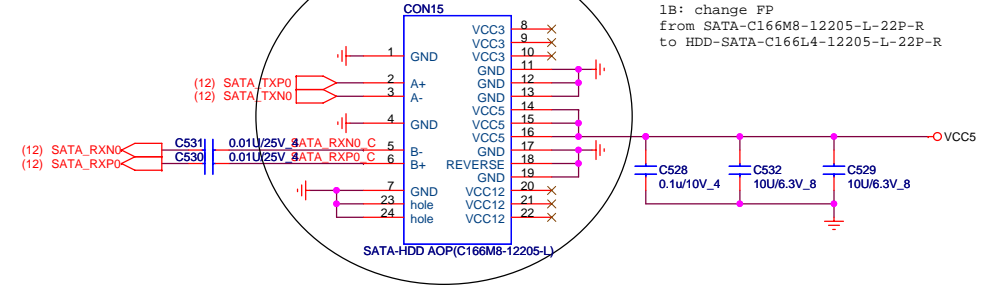
2A need check TOP or BOT again

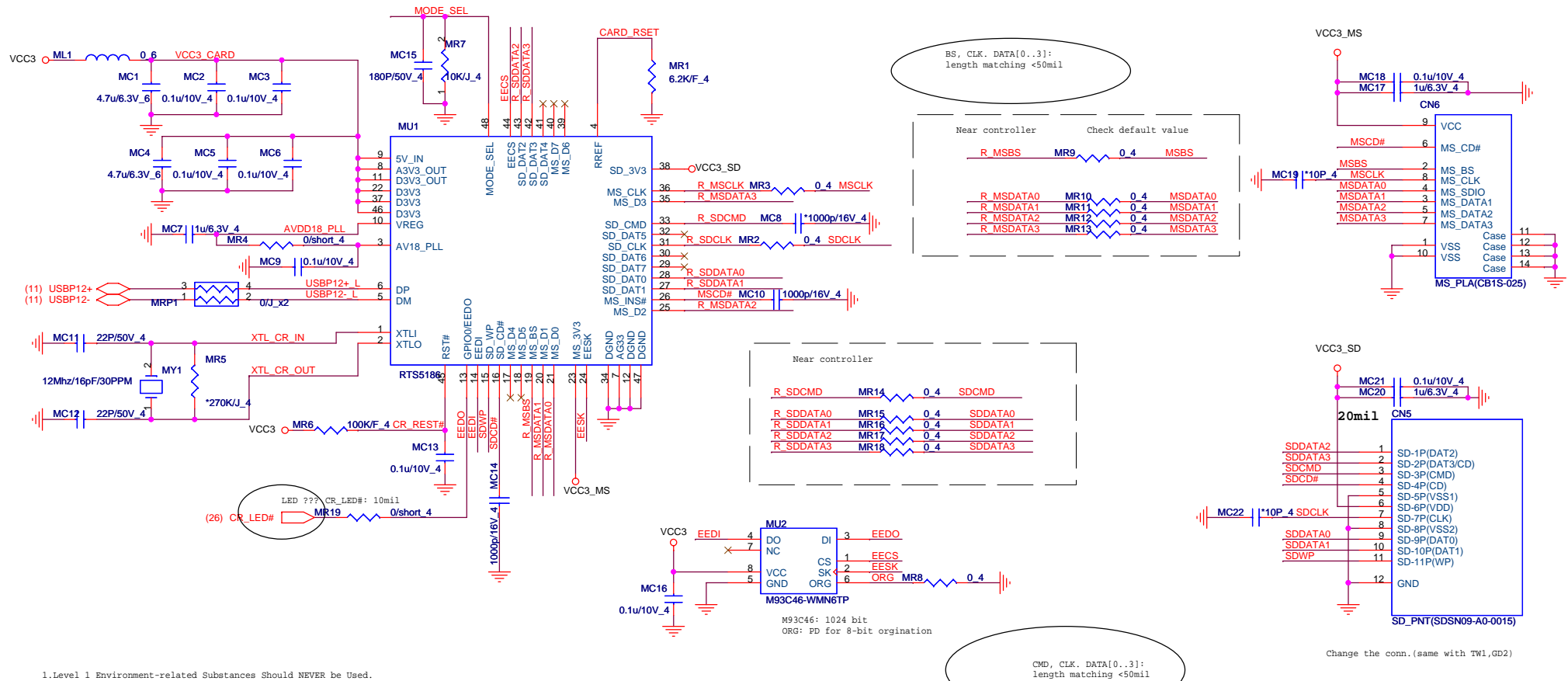


## SATA ODD



## 2.5 inch SATA HDD



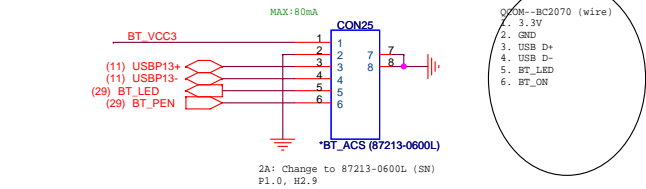
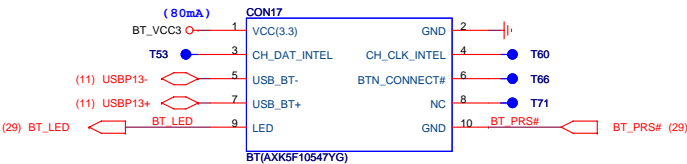
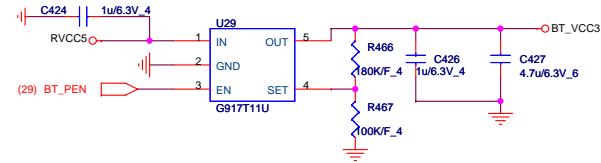


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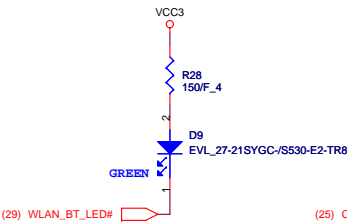
| Size  | Document Number             | Rev            |
|-------|-----------------------------|----------------|
|       | <b>CARD Reader</b>          | 2A             |
| Date: | Wednesday, January 27, 2010 | Sheet 25 of 42 |

2A : Remove Express card

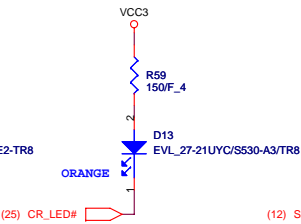
Bluetooth



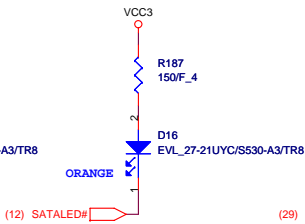
RF LED



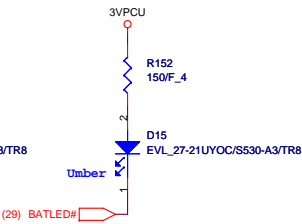
Card LED



HDD LED

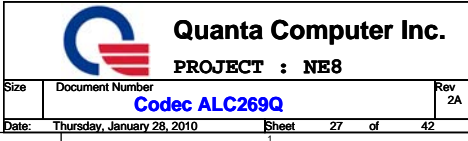


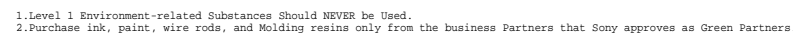
Battery LED



1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





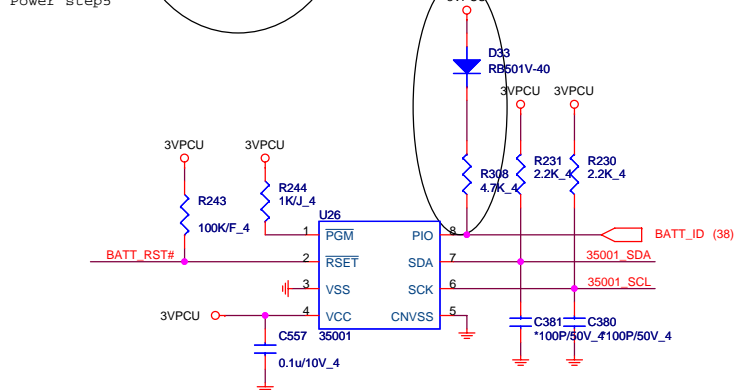
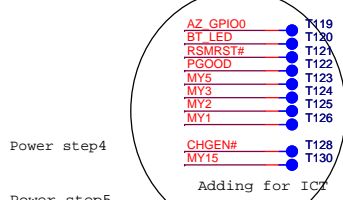
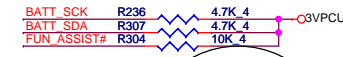
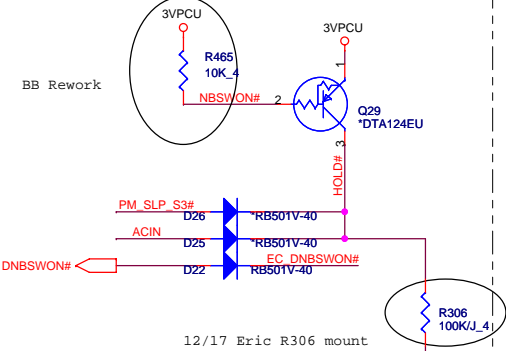


| I/O Address |                                             |      |
|-------------|---------------------------------------------|------|
| BADDR1-0    | Index                                       | Data |
| 1 0         | 2E                                          | 2F   |
| 1 1         | 4E                                          | 4F   |
| 0 0         | (HCFGBAH, HCFGBAL)   (HCFGGBAH, HCFGGBAL)+1 |      |
| 0 1         | XOR-Tree TEST                               |      |

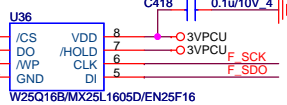
SHMB: SHMB(If = 0 Enable share host BIOS memory)

DOCK\_RST# : BADDR0  
T7: BADDR1

Reserved for more EC wake up function

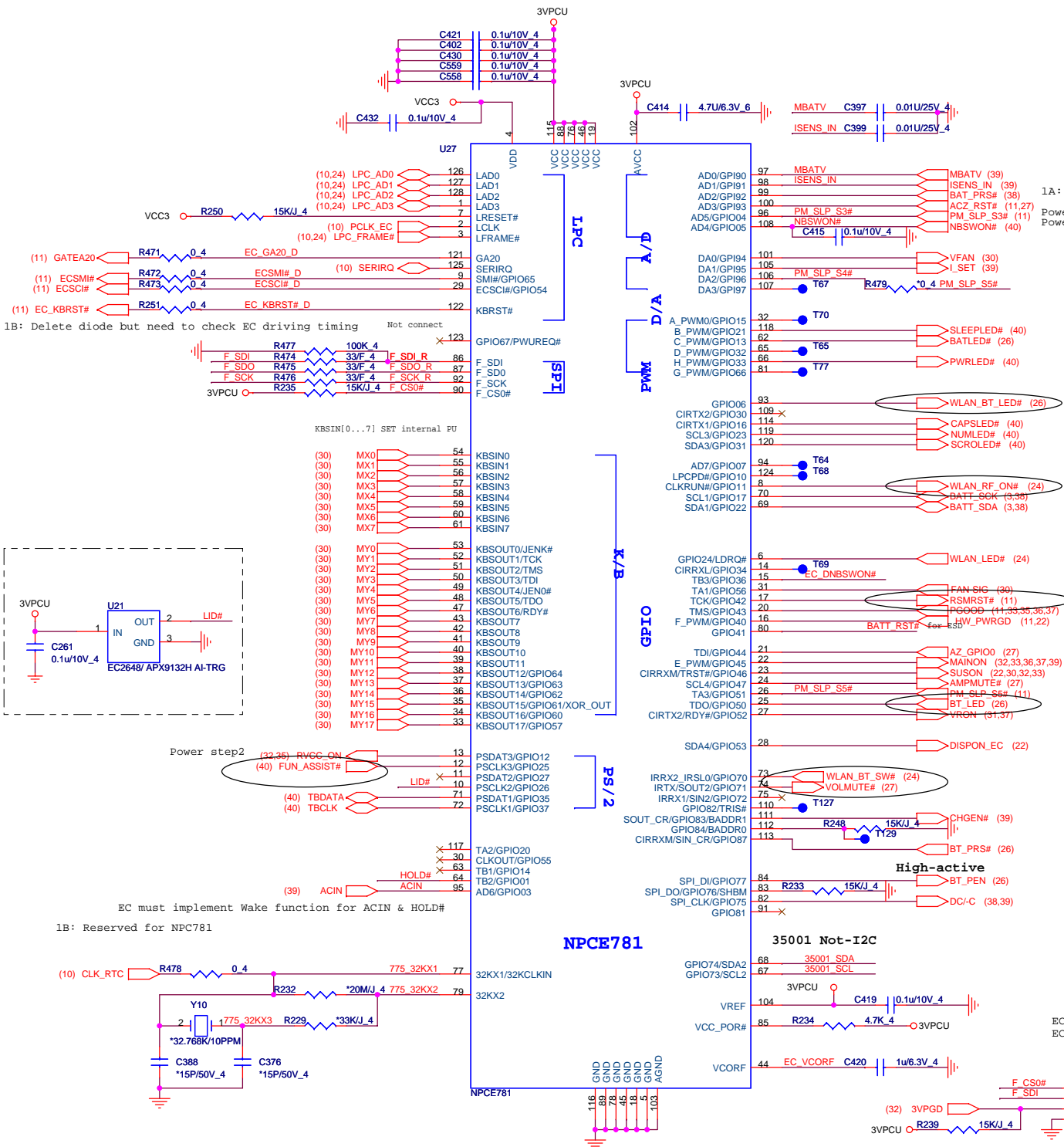


EC SDI-> EEPROM DO  
EC SDO-> EEPROM DI

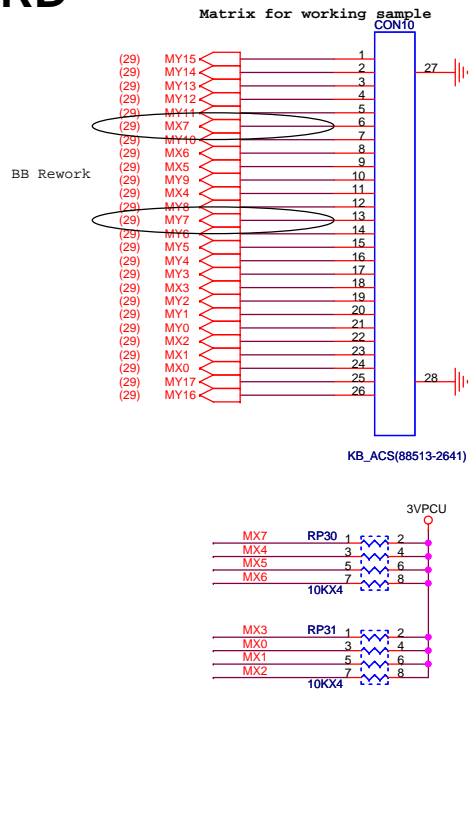


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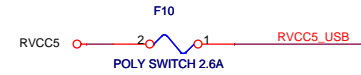
| Size  | Document Number             | Rev            |
|-------|-----------------------------|----------------|
|       | <b>NPCE781 &amp; FLASH</b>  | 2A             |
| Date: | Wednesday, January 27, 2010 | Sheet 29 of 42 |



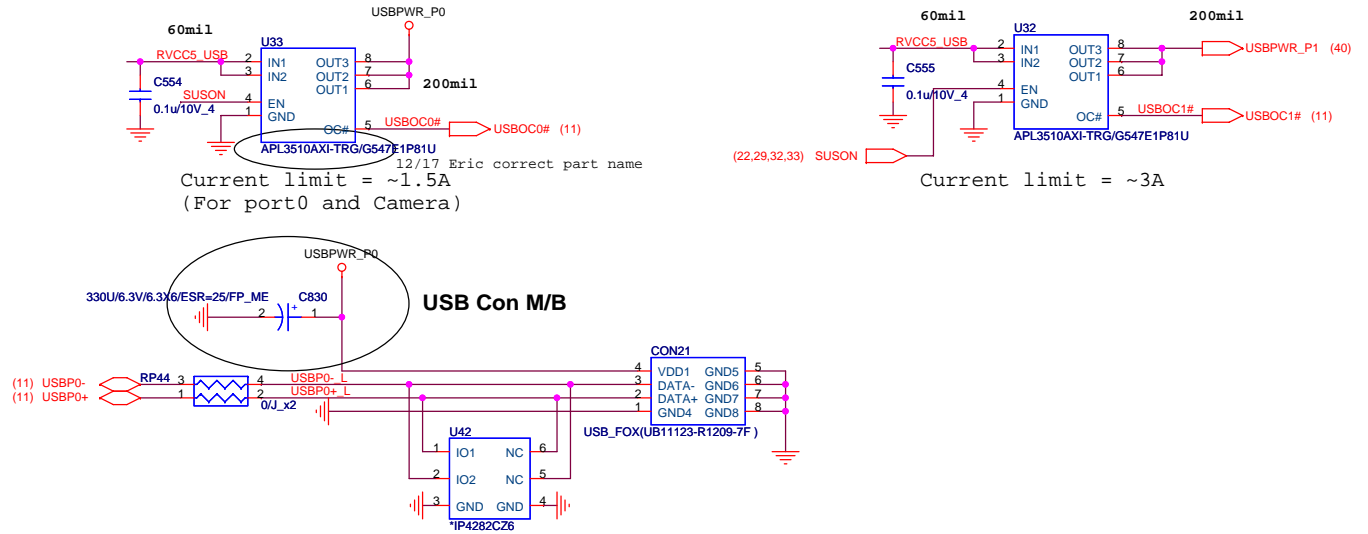
# KEYBOARD



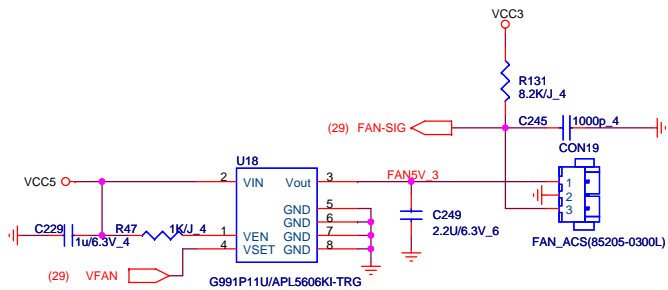
USB Port + e-SATA(USB)



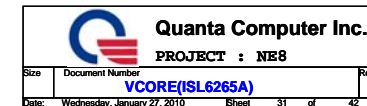
Current limit need to check

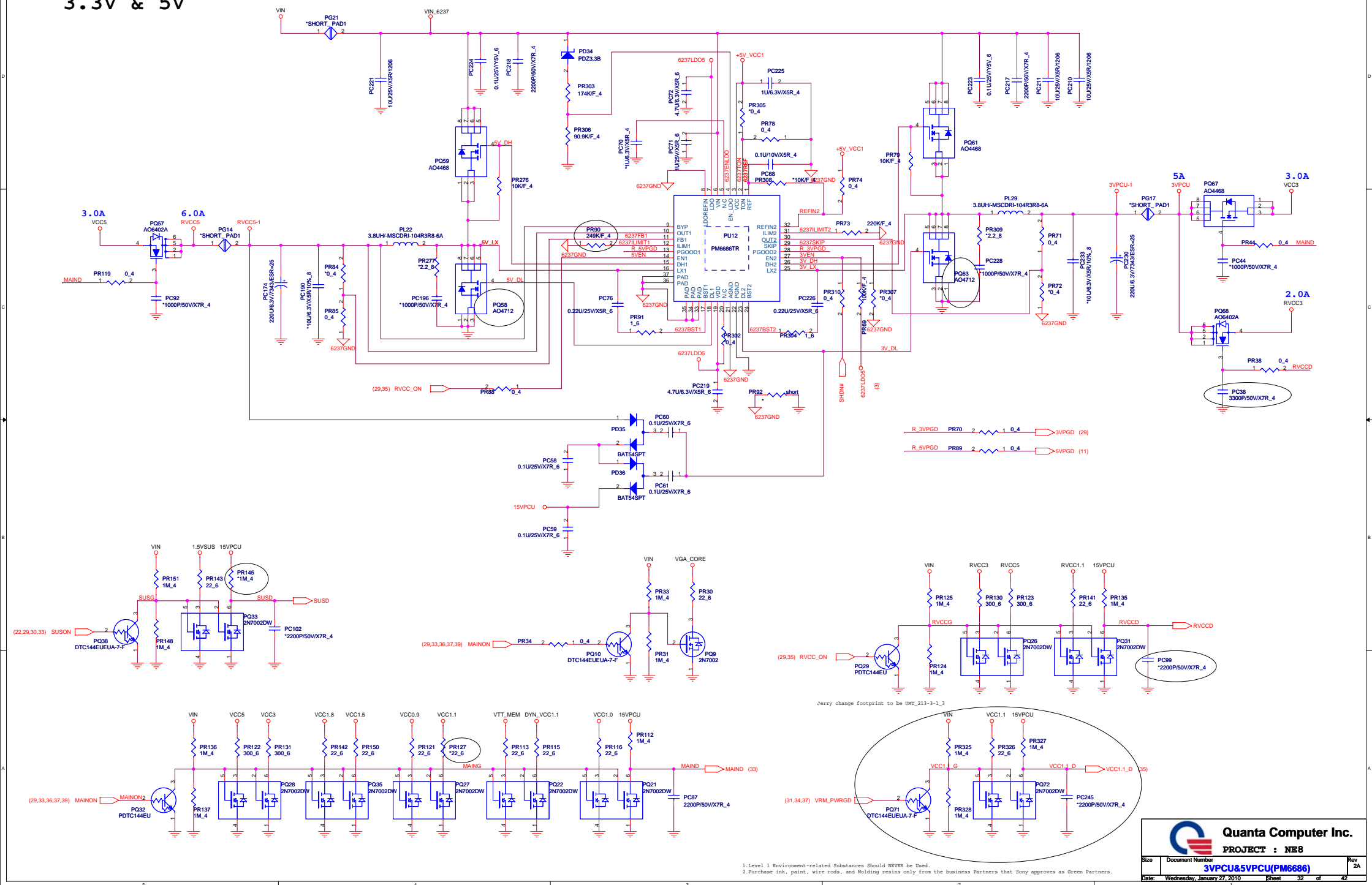


**FAN**



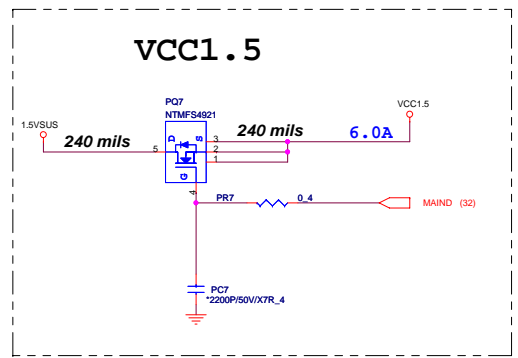
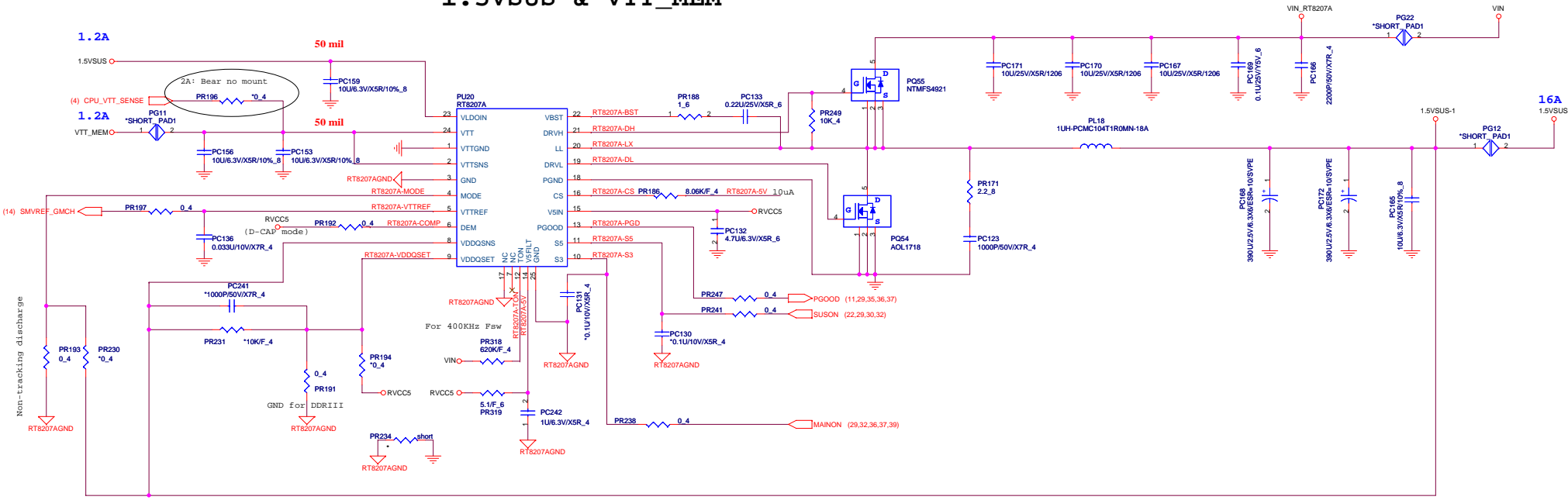
| SVC | SVD | Output |
|-----|-----|--------|
| 0   | 0   | 1.4    |
| 0   | 1   | 1.2    |
| 1   | 0   | 1.0    |
| 1   | 1   | 0.8    |







# 1.5VSUS & VTT\_MEM



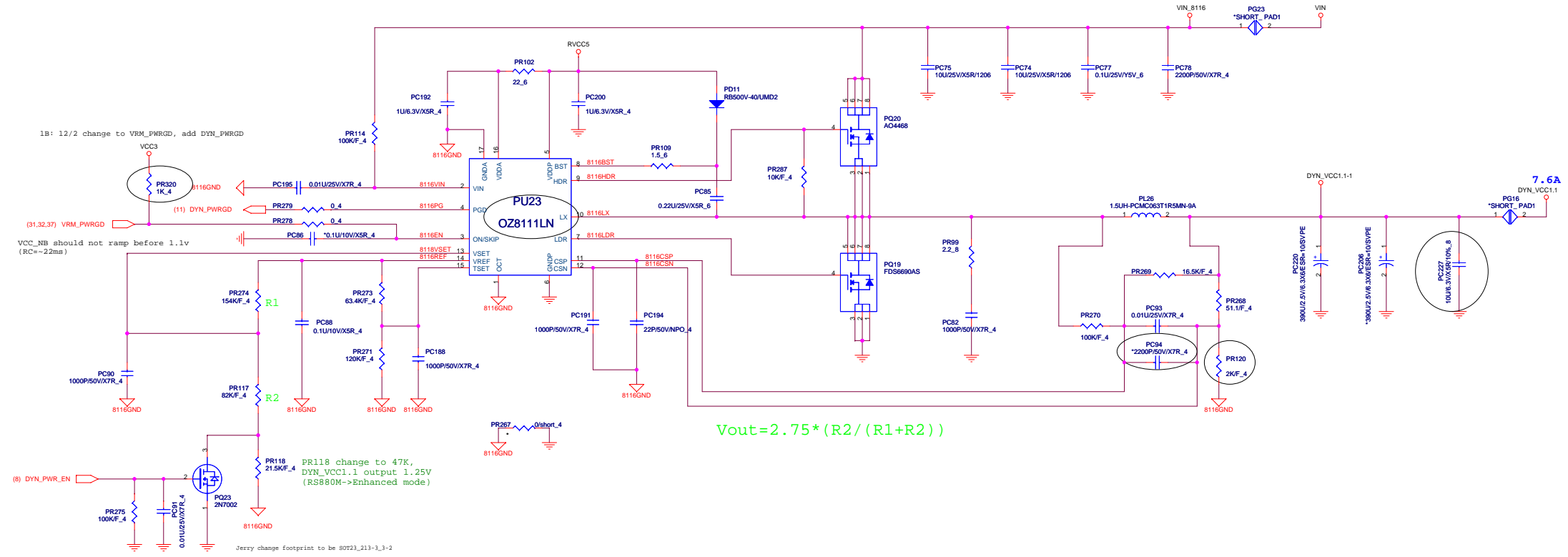
| MODE  | DISCHARGE MODE         |
|-------|------------------------|
| +5V   | No discharge           |
| +1.8V | Tracking discharge     |
| GND   | Non-tracking discharge |

| VDDQSET     | VDDQ(V)    | VTTREF & VTT | NOTE         |
|-------------|------------|--------------|--------------|
| GND         | 1.5 fixed  | VDDQNS/2     | DDR3         |
| 5V          | 1.8 fixed  | VDDQNS/2     | DDR2         |
| FB-Resistor | Adjustable | VDDQNS/2     | 1.5V<VDDQ<3V |

VTT = VTTREF = VDDQNS/2 = 0.75V

| STATE | S3 | S5 | 1.5VSUS | VTTREF | VTT |
|-------|----|----|---------|--------|-----|
| S0    | 1  | 1  | on      | on     | on  |
| S3    | 0  | 1  | on      | on     | off |
| S4/S5 | 0  | 0  | off     | off    | off |

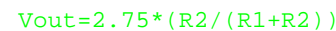
1.Level 1 Environment-related Substances should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



|            |       |      |
|------------|-------|------|
| DYN_PWR_EN | High  | Low  |
| DYN_VCC1.1 | 0.95V | 1.1V |

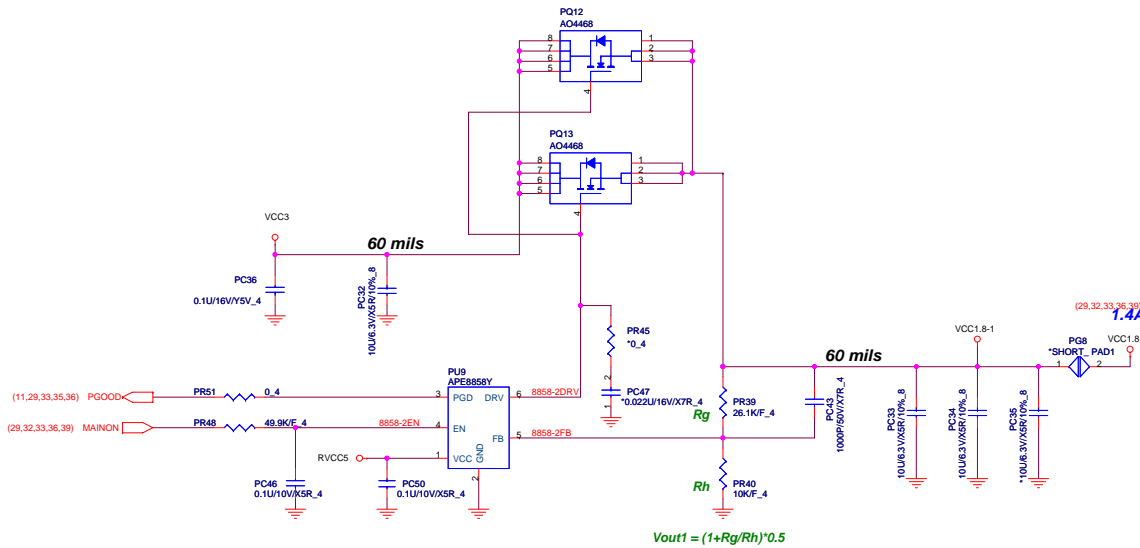
1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



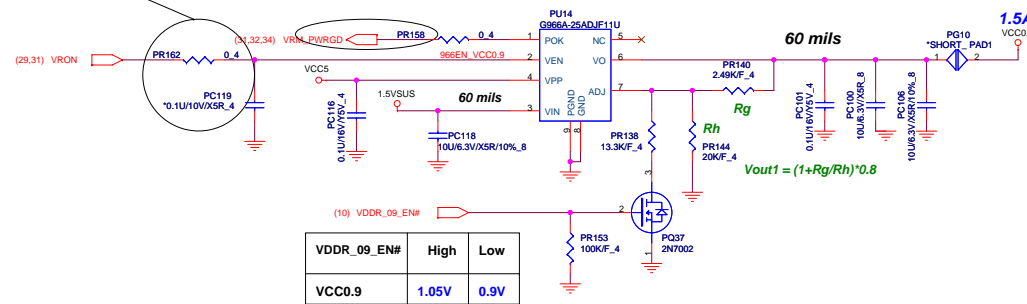


|            |          |
|------------|----------|
| V_PWRCNTL0 | VGA_CORE |
| 0          | 0.95V    |
| 1          | 0.90V    |

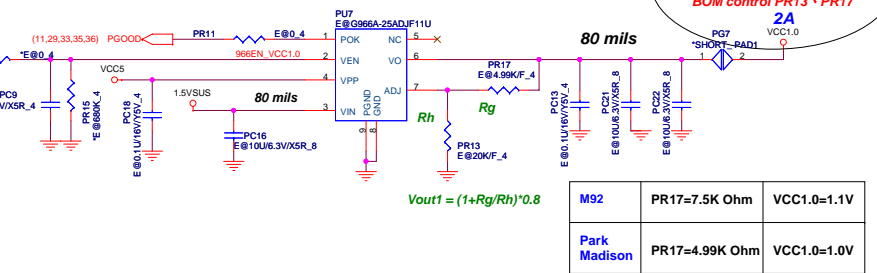
## VCC1.8



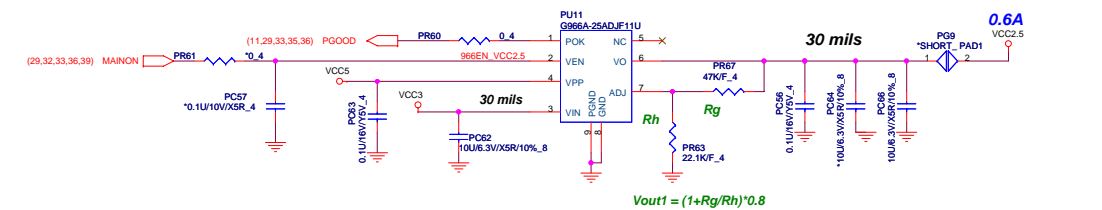
## VCC0.9



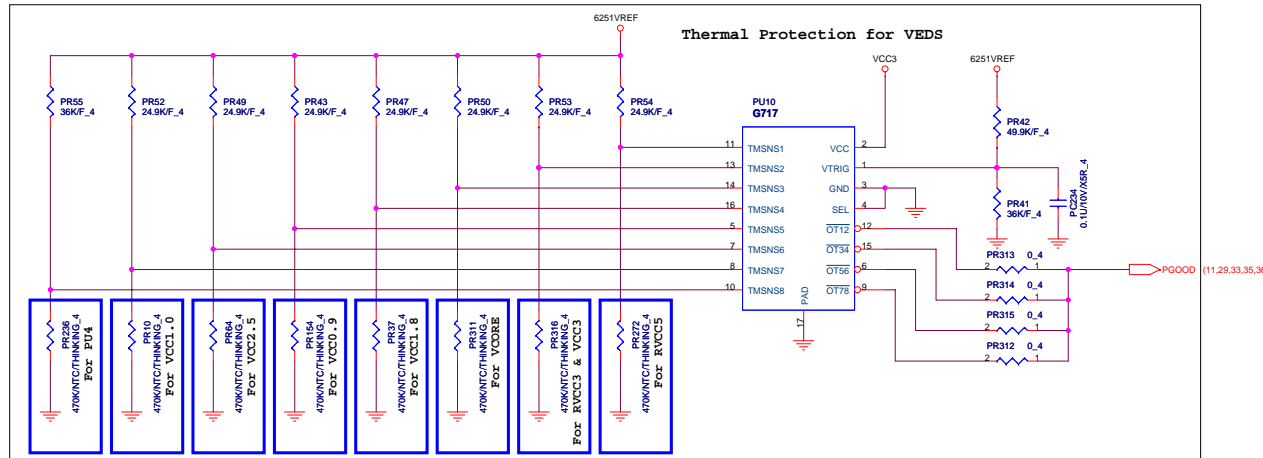
## VCC1.0

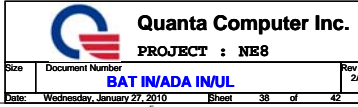


## VCC2.5



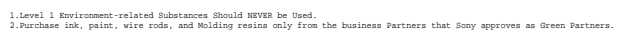
### Thermal Protection for VEDS

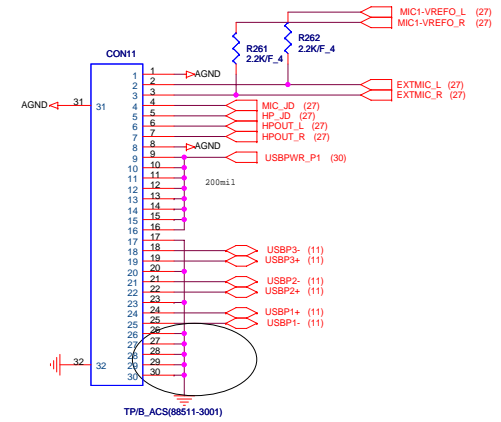
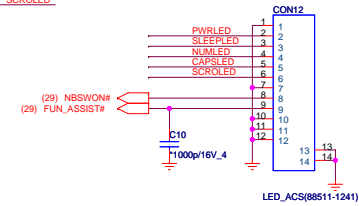
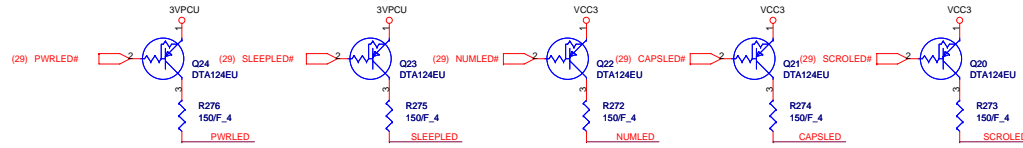
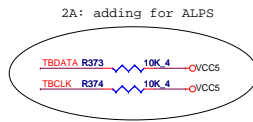
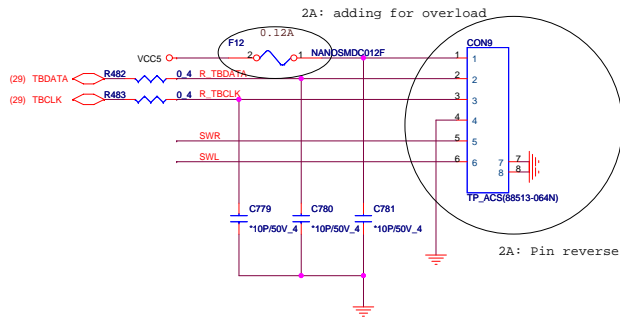
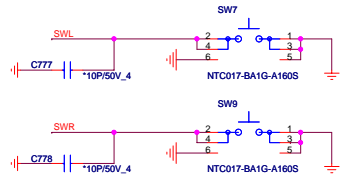




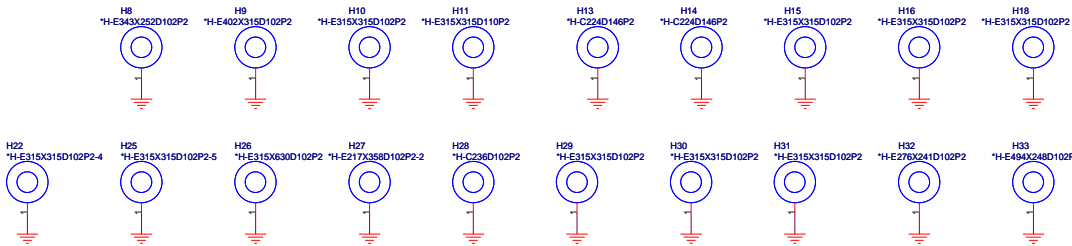
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners







2A: change CON11 form 26pin to 30pin.



WLAN

BT

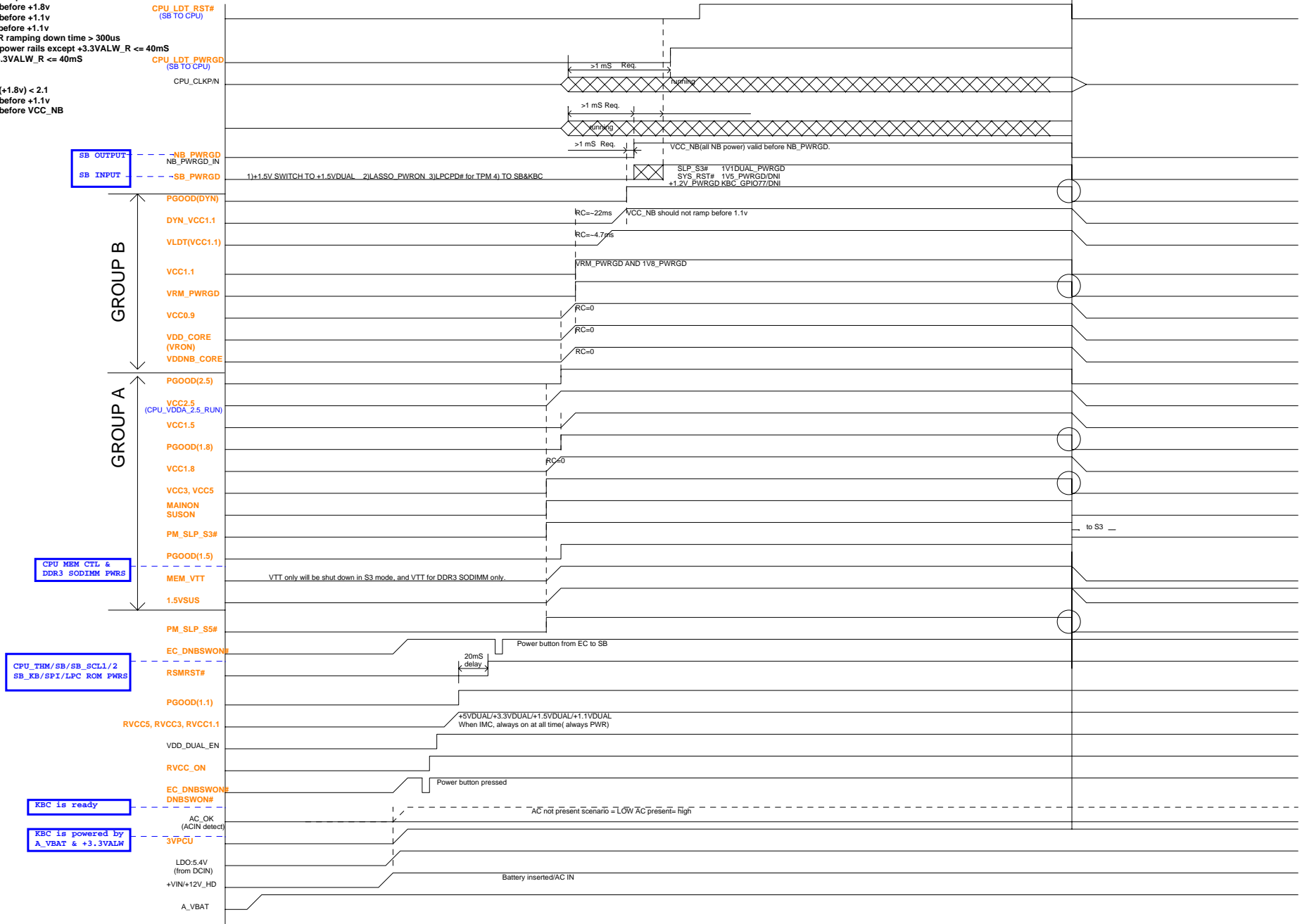
**Power on Sequence required:**

SB800:

- 1, +3.3VDUAL ramp before +1.1VDUAL
- 2, +3.3V ramp before +1.8v
- 3, +1.8V ramp before +1.1v
- 4, +3.3v ramp before +1.1v
- 5, +3.3VALW\_R ramping down time > 300us
- 6, 50uS <= All power rails except +3.3VALW\_R <= 40mS
- 7, 100uS <= +3.3VALW\_R <= 40mS


CPU  
(SB)  
CPU

**RS880:**  
 1,  $0 < (+3.3V) - (+1.8v) < 2.1$   
 2, +1.8V ramp before +1.1v  
 3. +1.1V ramp before VCC\_NB



2A Adding R159 (10K) for shut down issue.

1.Level 1 Environment-related Substances Should NEVER be Used.  
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Quanta Computer Inc.

PROJECT : NE8

|       |                             |                |
|-------|-----------------------------|----------------|
| Size  | Document Number             | Rev            |
|       | Change History              | 2A             |
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